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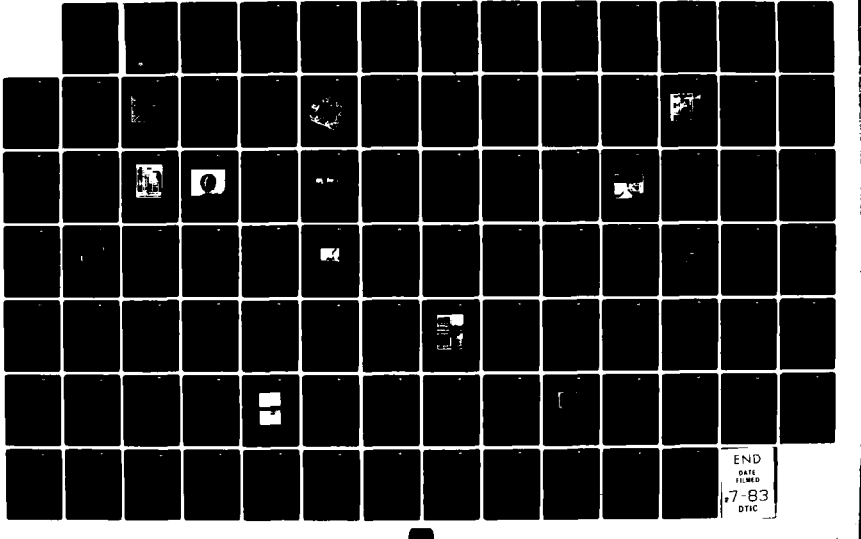

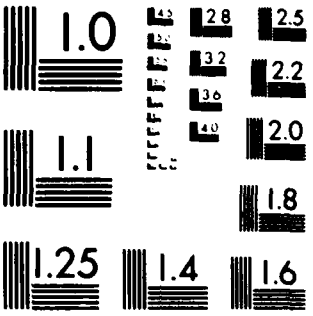

MONOLITHIC GALLIUM ARSENIDE SUPERHETERODYNE FRONT END

FINAL REPORT FOR THE PERIOD
August 15, 1978 through September 30, 1981

CONTRACT NO. N00014-78-C-0624

Prepared for

Office of Naval Research
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Arlington, VA 22217

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This final report describes the work performed under ONR Contract No. N00014-78-C-0624. The goal of the program was to develop GaAs monolithic microwave integrated circuitry (MMICs) for an 8 GHz superheterodyne receiver front end. The MMIC designs are based on microstrip circuitry fabricated on semi-insulating GaAs substrates with resistivity as high as 10^9 Ω/□. Single and two stage low noise amplifiers were successfully developed. An IF amplifier design was successful. Initial results were also obtained on a monolithic mixer and voltage controlled oscillator.

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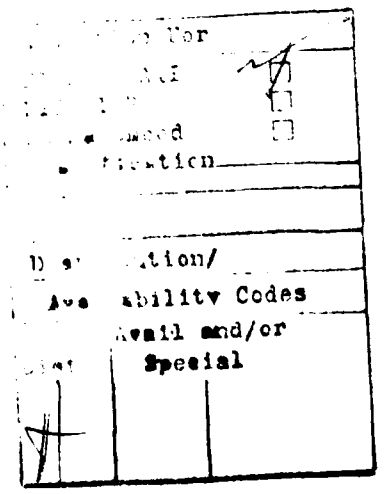
TABLE OF CONTENTS

		Page
	FOREWORD	1
1.0	INTRODUCTION	2
2.0	CIRCUIT DESIGN AND LAYOUT	3
	2.1 Performance Goals and Design Approach	3
	2.2 Initial Circuit Designs	6
	2.3 Circuit Design Improvements	19
	2.4 Analysis and Design for Low Noise	41
3.0	CIRCUIT FABRICATION TECHNOLOGY	44
	3.1 GaAs Materials and Ion Implantation Technology	46
	3.1.1 Semi-Insulating Substrate	46
	3.1.2 Profile Synthesis and Characterization	48
	3.2 GaAs MMIC Fabrication Technology	50
	3.3 Yield Considerations	58
	3.4 Circuit Fabrication Improvements for Low Noise	68
4.0	CHARACTERIZATION AND TEST RESULTS	73
	4.1 Measured Performance Results	73
	4.2 Characterization of Active Devices	84
	4.3 Performance Analysis	86
5.0	SUMMARY & RECOMMENDATIONS	87



LIST OF FIGURES

Figure		Page
2.1	Initial IF amplifier schematic circuit	7
2.2	SEM photograph of the initial IF amplifier chip. Chip size is approximately 2 × 2 mm^2	8
2.3	Calculated gain of IF amplifier	10
2.4	Photograph of circuit mounted in test fixture	11
2.5	Measured gain of the initial IF amplifier	12
2.6	Measured S_{11} and S_{22} of the initial IF amplifier	14
2.7	Circuit diagram of the initial 8 GHz RF preamplifier	15
2.8	Gain of the initial single stage RF preamplifier designed for a 7.75 to 8.25 GHz band	16
2.9	SEM photograph of the initial 8 GHz preamplifier chip. Chip size is 2.5 × 2.5 mm^2	17
2.10	Measured gain of the initial 8 GHz preamplifier	18
2.11	Measured input and output match of the initial 8 GHz preamplifier	20
2.12	Circuit diagram of the initial 8 GHz dual gate FET mixer	21
2.13	SEM photograph of the initial 8 GHz dual gate FET mixer. Chip size is approximately 2.5 × 2.5 mm^2	22
2.14	This photograph shows the initial RF preamplifier (left), FET mixer (center), and IF amplifier (right) on the face of a dime. The preamplifier and mixer are each 2.5 × 2.5 mm^2 and the IF amplifier is approximately 2 × 2 mm^2 in size	23
2.15	SEM of the improved IF amplifier	25
2.16	Effect of parasitic on preamplifier performance	27
2.17	Improved 8 GHz amplifier schematic	28
2.18	Predicted gain of improved single stage preamplifier	29

LIST OF FIGURES

Figure		Page
2.19	SEM photograph of improved single stage preamplifier.....	30
2.20	Schematic of two stage preamplifier.....	32
2.21	SEM photograph of two stage preamplifier.....	33
2.22	Schematic of improved 8 GHz mixer.....	34
2.23	SEM photograph of improved 8 GHz mixer.....	35
2.24	Voltage controlled oscillator schematic.....	38
2.25	SEM photograph of the oscillator chip.....	39
2.26	Reticle layout.....	40
3.1	Schematic diagram of a monolithic microwave integrated circuit.....	45
3.2	Ion implantation doping profiles in LEC and Bridgman semi-insulating GaAs substrates.....	51
3.3	A schematic diagram showing the nitride-aided lifting process. Si_3N_4 deposited on GaAs and the gate pattern is defined in positive photoresist on top. Exposed Si_3N_4 is etched in a plasma. Gate metal is then evaporated and lifted as usual.....	54
3.4	Photograph showing the excellent edge definition obtained with nitride-aided lifting. The two gates (~ 1 μm long) are spaced 1 μm apart in a 6 μm source-drain gap. Metal thickness is 5000A.....	55
3.4-1	W-Au gate with T shaped cross section.....	70
3.4-2	Recessed gate FET d-c characteristics.....	71
3.5	(a) Sharp corners obtained in attempting to define thick metal patterns by the lifting technique; (b) rounded corners obtained by chemically etching or ion milling the unwanted metal.....	57
3.6	Process evaluation chip.....	59

LIST OF FIGURES

Figure		Page
3.7	Typical pinchoff voltage uniformity obtained on one quarter of a 3-in. Cr-doped LEC substrate	60
3.8	Schematic diagram of a metal-insulator-metal (MIM) capacitor	64
3.9	(1) Sharp pattern edges obtained by direct liftoff of Ti(500A)/Au(4000A). (b) Smooth edges obtained by ion milling the metallization pattern	66
4.1	Measured gain of the improved IF amplifier	75
4.2	Measured input and output match of the improved IF amplifier	76
4.3	Measured preamplifier gain and noise figure without gate recess	77
4.4	Measured preamplifier input and output match	78
4.5	Measured preamplifier gain and noise figure with gate recess	79
4.6	Gain and noise figure of the two-stage buffer amplifier without gate recess	80
4.7	Input and output match of the two-stage buffer amplifier	81
4.8	Measured output return loss of the buffered local oscillator	83

LIST OF TABLES

Table		Page
2.4-1	Initial FET Noise Analysis	43
3.1-1	n-Type Implants Into GaAs with a Calculated Range of 1000A	49
3.3-1	Active Layer Uniformity	61
3.3-2	Specific Contact Resistance Results	62
3.3-3	MIM Capacitor Uniformity Data	63
3.3-4	DC Yield of MIM Capacitors	65
3.3-5	FET DC Yield	67
3.3-6	DC Circuit Yield	68
3.4-1	Effect of Surface N+ Layer	72

FOREWORD

This is the final report for ONR Contract No. N00014078-C-0624 which describes work performed between 15 August 1978 through 30 September 1981. The goal of this program is to develop GaAs monolithic microwave integrated circuitry (MMICs) for an 8 GHz monolithic superheterodyne receiver front end. The work described herein was carried out at the Rockwell International Microelectronics Research and Development Center, P.O. Box 1085, Thousand Oaks, CA.

The Program Manager and Principal Investi[illegible]or were Dr. D.R. Ch'en and Dr. D.R. Decker. Other members of the staff who have contributed to this program are: Drs. A.K. Gupta, W.C. Petersen, and J.A. Higgins. Mr. M.N. Yoder of the Office of Naval Research was the technical monitor of this program.

1.0 INTRODUCTION

This final report describes the work performed under ONR Contract No. N00014-78-C-0624 between 15 August 1978 and 30 September 1981. The goal of this program was to develop GaAs monolithic microwave integrated circuitry (MMICs) for an 8 GHz superheterodyne receiver front end for the satellite communications band. The MMIC designs are based on microstrip circuitry fabricated on semi-insulating GaAs substrates with resistivity as high as $10^9 \Omega/\square$. Active devices, bias networks, and microwave circuitry are integrated to realize a fully monolithic microwave technology. Ion implantation doping technology facilitates control of doping density and profile for optimization of active device characteristics and achievement of high circuit fabrication yields.

The monolithic receiver circuitry fabricated under this program comprises a single-stage low-noise amplifier, a two-stage low-noise amplifier, a FET mixer, an IF amplifier and a voltage-controlled local oscillator circuit. These circuits were all built on a common mask set using a multi-cell reticle approach which also included a process monitoring and test pattern as one of the 6 reticle cells.

This report is organized as follows. Section 2.0 describes the program goals and design approach, initial circuit designs, design improvements, and analysis and design for low noise. A discussion of the GaAs MMIC materials and fabrication technology is contained in Section 3.0 which also describes yield considerations and low-noise device fabrication improvements. Test results and performance analysis are discussed in Section 4.0. Finally, Section 5.0 provides a summary and recommendations for further work to upgrade individual circuit performance and complete full monolithic receiver integration.

2.0 CIRCUIT DESIGN AND LAYOUT

This section describes performance goals for the 8 GHz Monolithic Superheterodyne Receiver Front End and the design approach utilized to meet these goals. Integrated circuit design consists of an initial circuit concept, optimization, layout, fabrication, measurement, and data analysis followed by one or more iterations to refine the measured performance and approach the design goals. Initial iterations of the superheterodyne receiver component parts have been described in interim reports for this program and in the final report for ONR Contract N00014-79-C-0726 entitled "Monolithic GaAs Oscillator Development." The initial designs and results are summarized for completeness in addition to the detailed description of more recent circuit designs. Measured performance of the latest designs is presented in Section 4.0. This section concludes with a review of the analysis and design techniques necessary for the successful design and fabrication of low noise GaAs integrated circuits such as the 8 GHz receiver front end.

2.1 Performance Goals and Design Approach

The goal of this program was the development of a Monolithic Superheterodyne Receiver Front End. Performance goals for the receiver front end were:

Frequency:	7.5 to 8.25 GHz
RF to IF gain:	30 dB min.
Noise Figure:	3.9 dB max.

In order to realize this goal in an expedient manner, the design approach selected was to first design, fabricate, and characterize the individual receiver component parts prior to the integration of the receiver chip. The component parts of the receiver are a two stage buffer amplifier, a mixer, a stabilized local oscillator, and an intermediate frequency amplifier. A one stage buffer amplifier was developed in the process of designing the two stage

buffer amplifier. The second design iteration then provided the ability to test each component individually or to test an entire receiver by the addition of a few short interconnecting bond wires. This capability was achieved by careful layout of each component circuit and proper reticle configuration. Interfaces between circuits were all at a 50 ohm impedance level to facilitate separate component testing.

To meet the overall receiver goals, the following goals were placed on each of the component parts:

Preamplifier:

Gain:	8 dB per stage
Noise Figure:	3.1 dB (single stage)
	3.4 dB (two stage)

Mixer:

Conversion Gain:	8 dB
Noise Figure:	8 dB

IF Amplifier:

Gain:	10 dB
Noise Figure:	6 dB

Oscillator:

Output Power:	10 dBm
External Phase Lock	Capability

As described in the following sections, the gain of the preamplifier will roll off as a function of frequency when tuned for optimum noise figure. Assuming a high side local oscillator, the IF amplifier was designed with a similar gain slope to provide receiver gain compensation.

One of the most important considerations in the selection of a design approach for monolithic integrated circuits is the compactness of the final circuit. A small circuit is essential for high yield, mechanical strength, potential low cost, and the potential of further integration into larger subsystems. Therefore, microstrip circuitry was selected as the transmission medium over coplanar transmission lines, slot lines, and other space consuming modes of transmission. Microstrip also simplifies the testing and packaging since a good ground plane is available on the chip back surface, which also provides a convenient heat sink (not of primary importance in this application due to the low power dissipation of the monolithic components utilized in the receiver front end). The thickness of the GaAs is then selected as a compromise between conflicting requirements. A thick substrate is desired to obtain a high maximum transmission line impedance, low loss, low parasitic capacitance to the ground plane, and mechanical strength. A thin substrate provides low coupling between adjacent transmission lines for small size, and an improved heat sinking capability. The need for low impedance transmission lines is substantially reduced by the availability of lumped metal-insulator-metal capacitors. A substrate thickness of 635 microns (25 mils) was selected in the initial designs, however, this was reduced to 250 microns (10 mils) in the later design iterations. A maximum transmission line impedance of approximately 100 ohms (15 microns wide on 250 micron thick GaAs) allows implementation of each component circuit on a 2 mm × 2 mm GaAs chip. The overall receiver front end (all four component parts) then occupies approximately 16 square millimeters.

A major consideration in the design was the need for accurate and comprehensive computer modeling of each circuit component and the composite circuit layout. All designs are iterative in nature and it is essential to do as many of the iterations as possible by computer modeling as opposed to the expensive and time-consuming sequence of mask fabrication, device fabrication, and device evaluation. Circuit models include all active and passive component models as well as all interelement parasitic coupling due to the layout. Each change in component value or chip layout must be evaluated to ensure that RF performance is not compromised as the final circuit configuration evolves. The

importance of this aspect of the design process is emphasized by the performance of the first circuits developed. Further evaluation and upgrading the computer models accordingly, provided the data base necessary for successful second iteration designs. A similar evolution of processing techniques occurred throughout this program as described in Section 3.0.

2.2 Initial Circuit Designs

The initial 8 GHz amplifier, mixer, and intermediate frequency amplifier were designed for fabrication on 635 micron thick GaAs used as a dielectric for microstrip circuitry. The oscillator was designed under a separate contract at a later date. This section describes the initial circuit designs and test results. Fabrication details are presented in Section 3.0. Section 2.3 will describe the improvements deemed necessary for full performance operation, and measured performance of the improved circuits is described in Section 4.0.

The IF amplifier was designed to be compact and to contain on chip biasing circuitry. The compact design was made possible by elimination of inductive matching elements. The amplifier was designed using the commercially available COMPACT CAD program. The dual-gate FET was modeled using an equivalent circuit composed of single-gate FET equivalent circuits in the common source and common gate connection. A circuit diagram of the IF amplifier is shown in Fig. 2.1 and an SEM photograph of the circuit fabricated on GaAs is shown in Fig. 2.2.

RF grounding of the active devices is accomplished with top surface ground planes along each edge of the chip. At the IF frequencies, grounding inductance is quite acceptable with this approach. Input and output of the IF amplifier are via 50 Ω transmission lines which are isolated by metal-insulator-metal (MIM) coupling capacitors (10 to 20 pF). Bias lines are provided for each of the FET gates and for V_{dd}. All bias lines are bypassed by MIM capacitors of 7 to 12 pF in value. An interdigital coupling capacitor of value 0.6 pF is used to couple the output of the dual gate FET to the gate of the source follower output stage and simultaneously provide dc bias isolation. The high impedance

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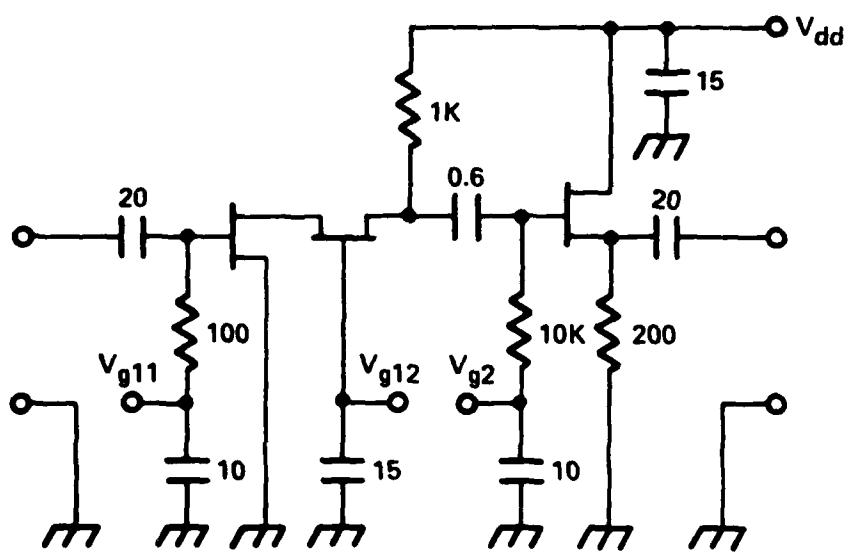

Fig. 2.1 Initial IF amplifier schematic circuit.

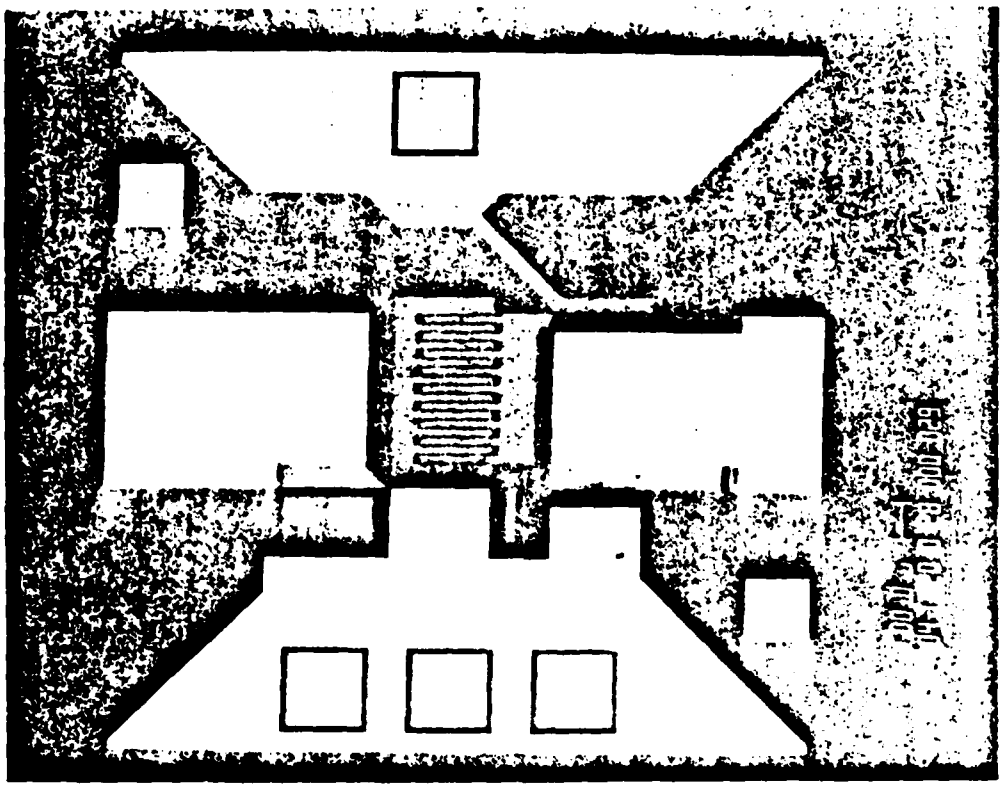

Fig. 2.2 SEM photograph of the initial IF amplifier chip. Chip size is approximately 2 × 2 mm^2.

at this point permits the usage of a relatively small coupling capacitor at low frequencies.

Since the noise figure of the IF amplifier will be buffered by at least 20 dB of gain from the preceding preamplifier and mixer, the noise performance was not a primary design concern. The amplifier was designed to provide a nominal gain of 10 dB between 500 and 1000 MHz as shown in Fig. 2.3. The input match to 50 Ω is required for testing convenience only and is determined by a shunt 100 Ω resistor to ground to be about 2:1 VSWR. This resistor is not necessary in the integrated version of the receiver front end. An excellent output match to 50Ω is obtained with active matching by using an FET in the common drain connection. In this configuration, the output impedance is approximately equal to the inverse of the FET transconductance. Thus a transconductance of about 20 mS is appropriate for matching to a 50 Ω line. A 200 Ω shunt resistor is used at the output for biasing the source of the output transistor.

Completed circuits are mounted into a microstrip test fixture as shown in the photograph of Fig. 2.4. The circuit is bonded between two alumina microstrip circuits which carry connections for input and output transmission lines and bias leads. In the IF frequency range this test fixture has been characterized to have less than 0.2 dB insertion loss with VSWR less than 1.07:1 at input and output (>30 dB return loss). The test fixture is connected to the measurement system using SMA type connectors. Bias is applied at the four screw terminals which are additionally bypassed with 1 μF ceramic capacitors.

The monolithic IF amplifier has been characterized for gain, isolation, and input and output match across the band from 500 to 1500 MHz. The measured gain is compared to the predicted gain in Fig. 2.5. As may be seen from the figure, the measured gain is about 3 dB below the predicted gain at 500 MHz and about 4 dB below the predicted curve at 1000 MHz. The lower gain and increased gain slope can be attributed to parasitic capacitances associated with the relatively large size of the interdigital coupling capacitor which were not included in the initial circuit design. The calculated gain including these additional

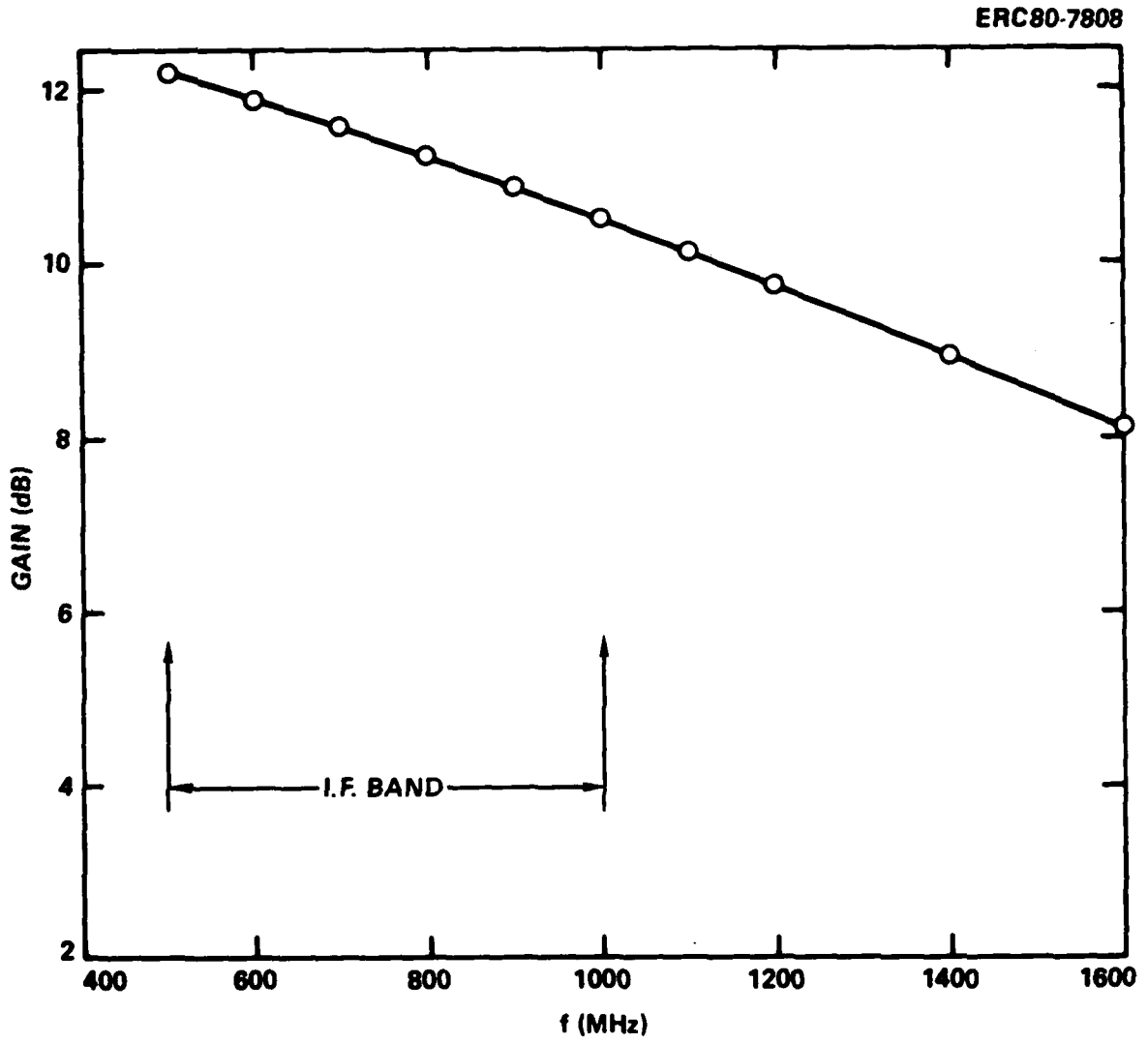

Fig. 2.3 Calculated gain of IF amplifier.

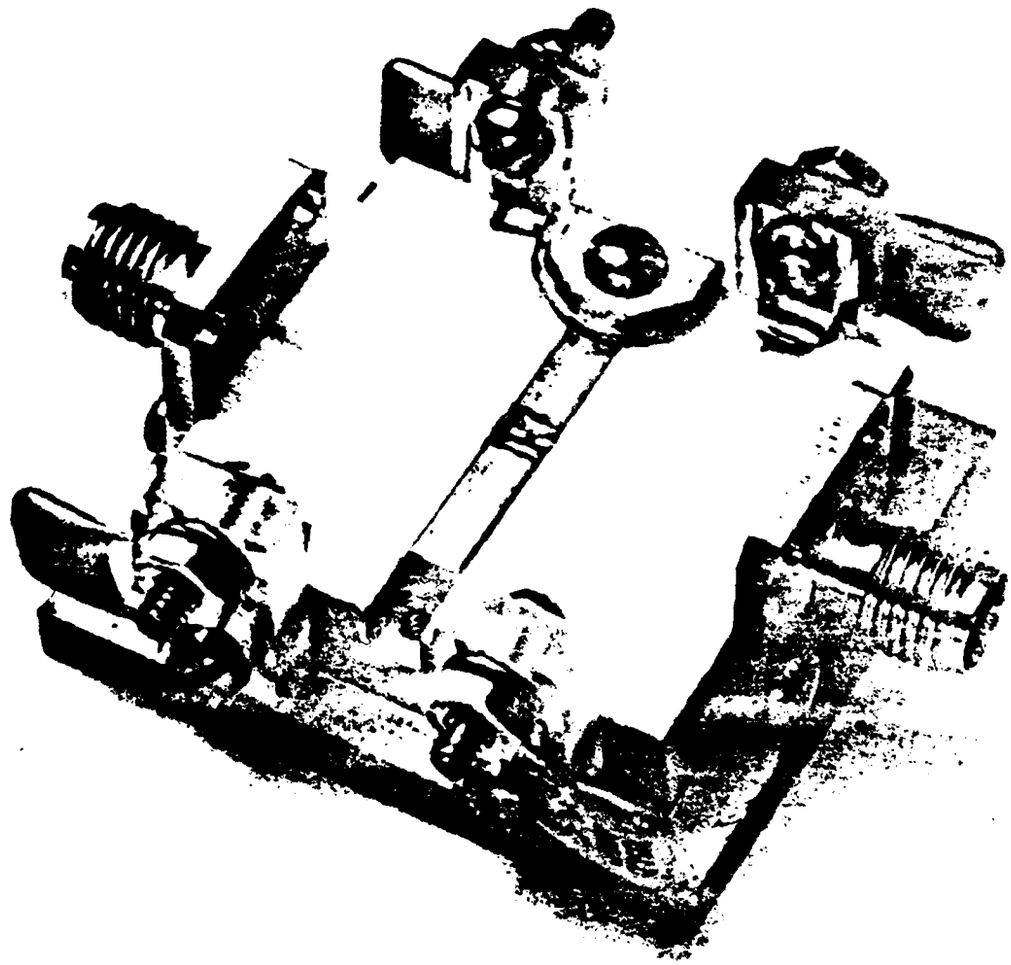

Fig. 2.4 Photograph of circuit mounted in test fixture.

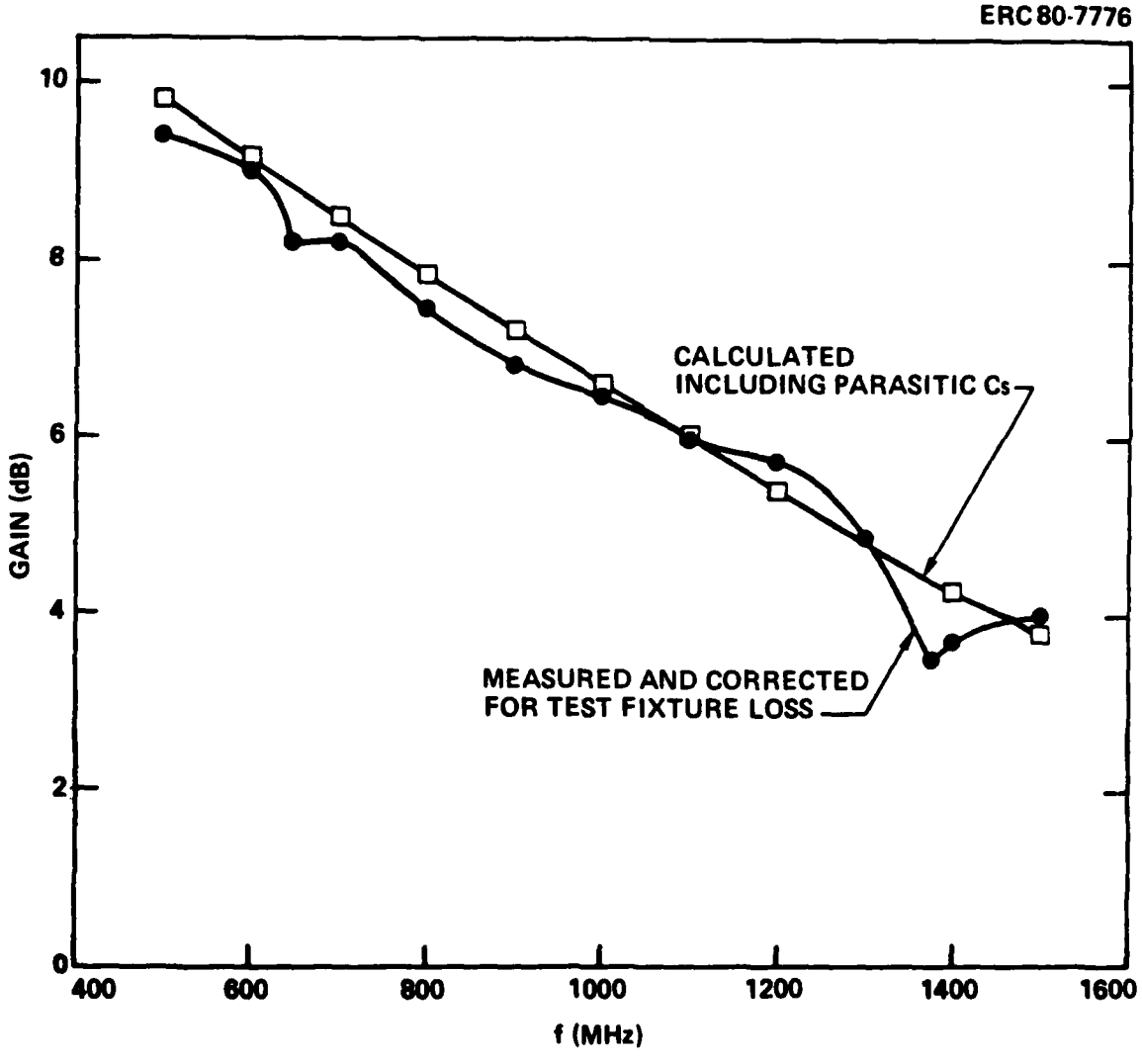

Fig. 2.5 Measured gain of the initial IF amplifier.

parasitics is seen to closely predict the observed performance. These parasitics were minimized through reconfiguration in the second version of this circuit as described in Section 2.3.

The input and output return loss measured for the initial IF amplifier design are shown in Fig. 2.6. The input VSWR is determined primarily by the 100 Ω shunt resistor, the 7.5 pF bypass capacitor, and 20 pF isolation capacitor in the input network. The input return loss is about 3 dB smaller than predicted which may be attributed to a reduced value for the bypass capacitor from 10 pF to 7.5 pF in the mask layout. Since, as previously mentioned, the input match is not a primary concern for this amplifier, this result is satisfactory. The output match obtained using the source follower configuration is very good across the band from 500 to 1000 MHz as seen in Fig. 2.7. Output return loss is better than about 15 dB between 800 and 1500 MHz (except at 1100 MHz) dropping to about 10 dB at 500 MHz. The reduction of output return loss near the low end of the band may again be attributed to somewhat low values of bypass capacitors.

Noise figure of the IF amplifier was tested across the 500 to 1000 MHz band. The measured noise figure was 8 dB across the band which, when corrected for the noise of the 100 Ω shunt resistor (which will not be present in the final configuration) gives an amplifier noise figure of about 6.25 dB. Noise tuning of the interstage matching could be used to reduce these values when this amplifier is integrated with the mixture circuit. However, such tuning will probably not be necessary since the expected 20 dB gain of the preamplifier and mixer reduce the noise contribution of the IF amplifier to less than 0.1 dB at its present performance level.

A schematic diagram of the initial preamplifier design is given in Fig. 2.7. This design uses a 300 μm wide GaAs FET with a 1 μm long gate. It was designed to provide ~ 8 dB gain over the 7.75 - 8.25 GHz band as shown in Fig. 2.8. An SEM photograph of the 2.5 × 2.5 millimeter chip is shown in Fig. 2.9.

Measured gain of this amplifier chip was obtained by mounting the chip in the test fixture shown in Fig. 2.4. The gain obtained is shown in Fig. 2.10

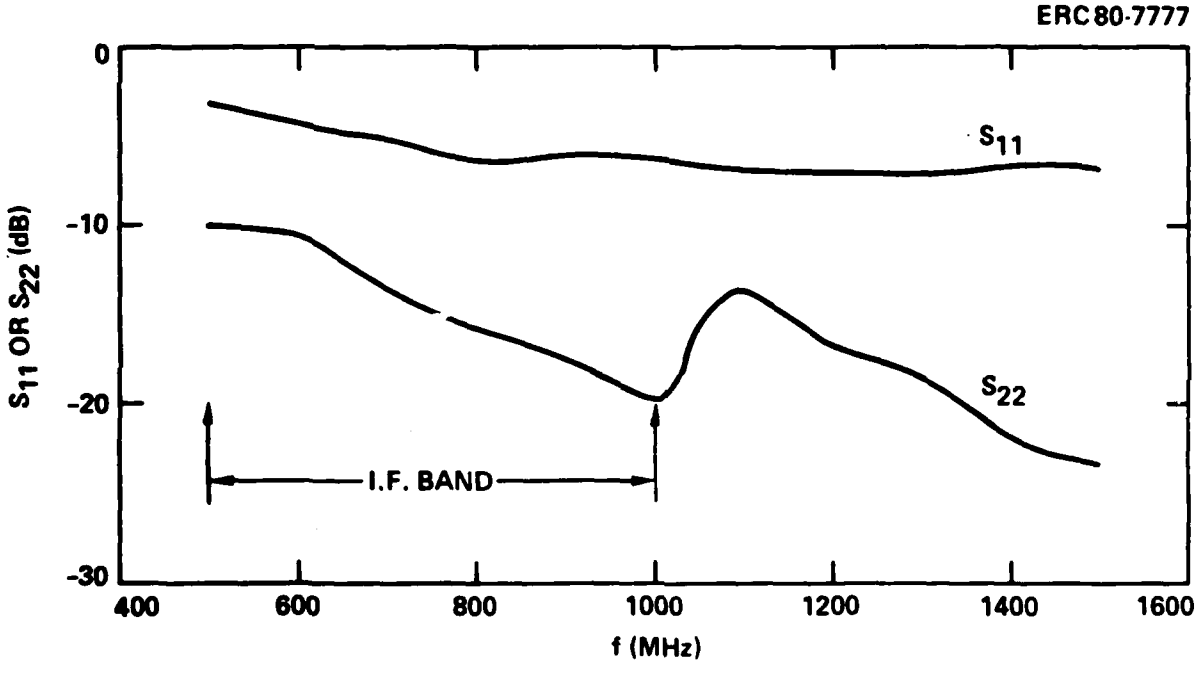

Fig. 2.6 Measured S_{11} and S_{22} of the initial IF amplifier.

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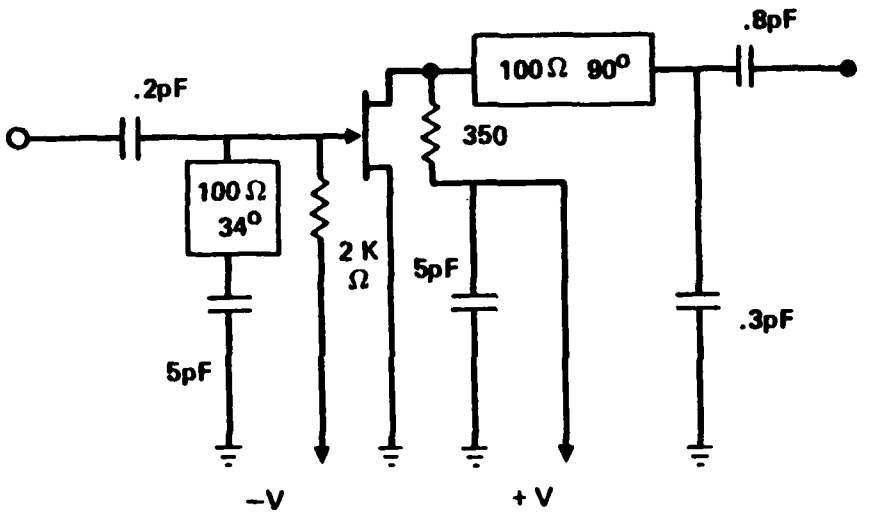

Fig. 2.7 Circuit diagram of the initial 8 GHz RF preamplifier.

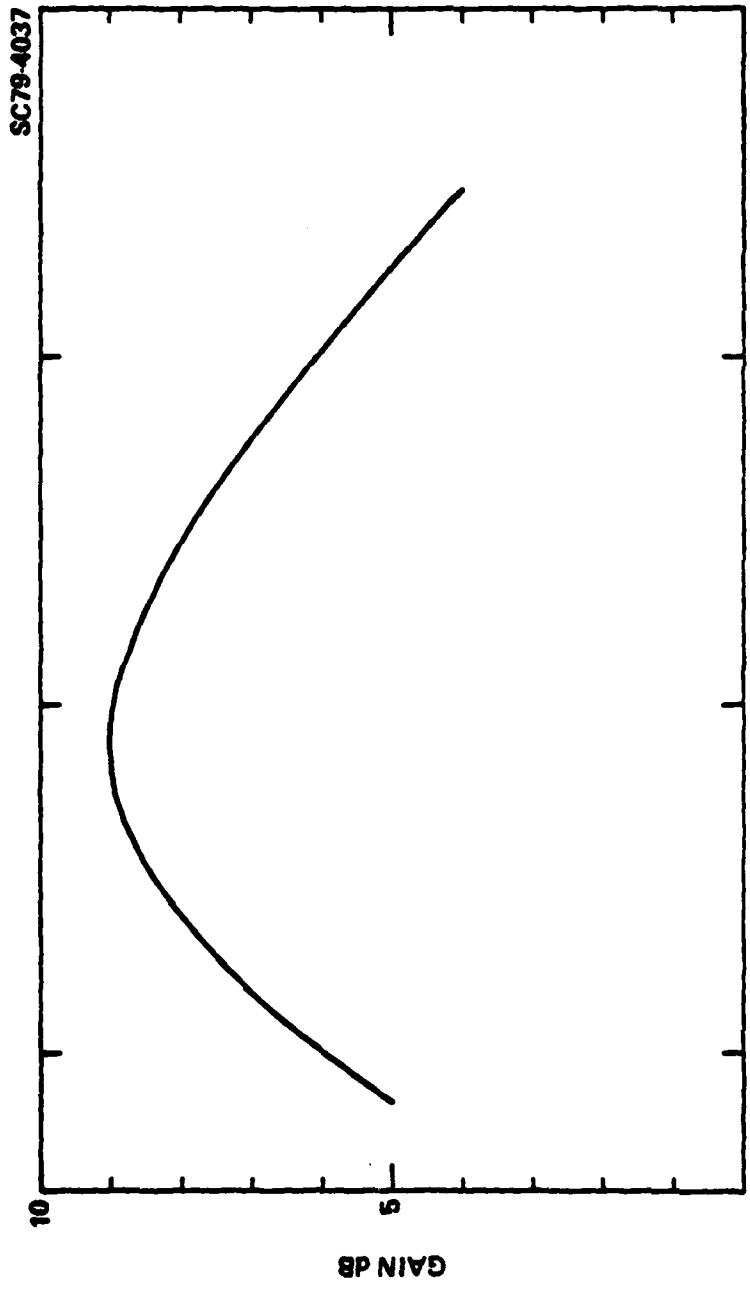

Fig. 2.8 Gain of the initial single stage RF preamplifier designed for a 7.75 to 8.25 GHz band.

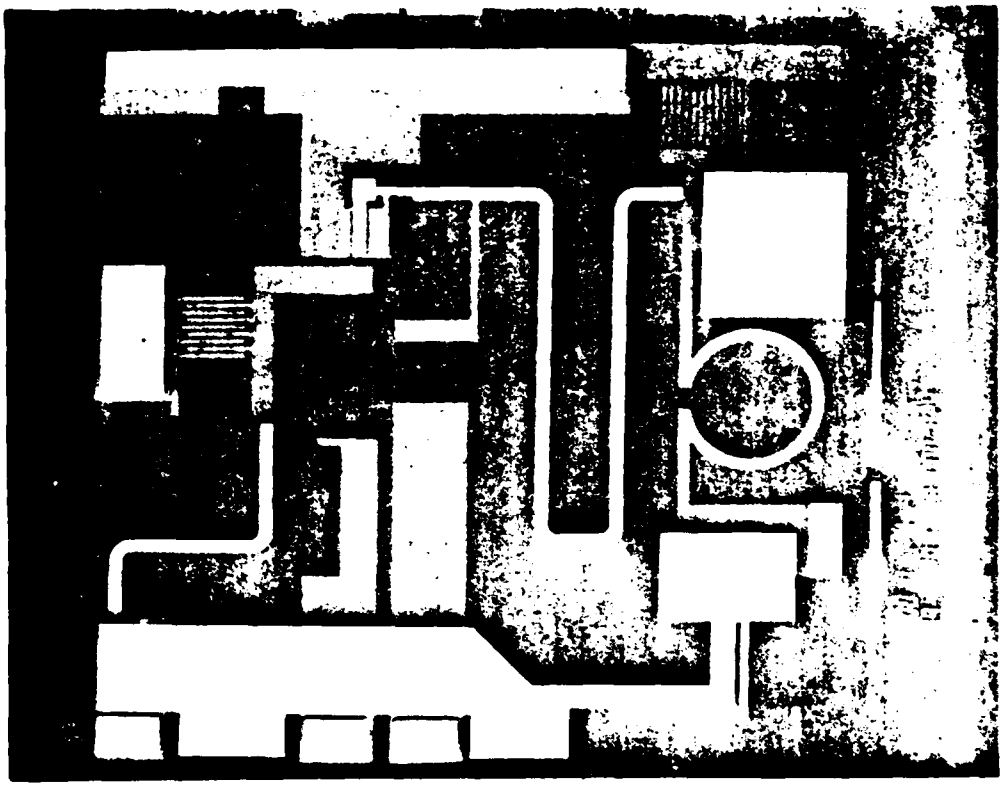

Fig. 2.9 SEM photograph of the initial 8 GHz preamplifier chip. Chip size is 2.5 × 2.5 mm^2.

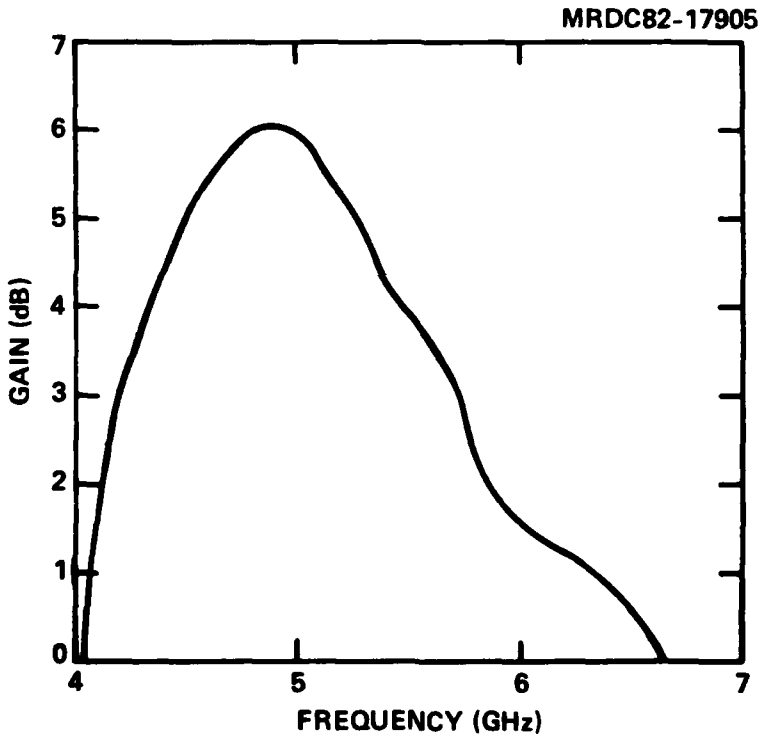

Fig. 2.10 Measured gain of the initial 8 GHz preamplifier.

while the input and output match is shown in Fig. 2.11. The lower than expected frequency of operation was the result of insufficient parasitic element modeling. These modeling deficiencies were corrected in the newer circuits described in Section 2.3.

A circuit diagram of the initial dual gate FET mixer is shown in Fig. 2.12. This design incorporates a 500 μm wide dual gate FET for mixing and a 300 μm wide FET at the IF output port. The predicted gain of this circuit measured from the signal gate to the output is of a low pass nature, giving +15 dB of gain at 1 GHz, and -7 dB at 8 GHz. The output transistor is connected in the source follower configuration. The high input impedance of this stage is a necessary component of the low pass nature of the drain circuit of the dual gate FET. It also provides a 50 Ω output impedance at the IF frequency. Figure 2.13 is an SEM photograph of an actual circuit. This circuit also uses a 635 μm thick GaAs substrate, microstrip transmission lines, and a top surface ground plane for grounding of active and passive elements. All bias lines are bypassed with integral MIM capacitors.

Bandwidth of this mixer was extremely narrow due to insufficient parasitic element modeling, however, a spot frequency measurement produced a conversion gain of 2 dB near 8 GHz with an IF output at 300 MHz.

The three initial circuits developed under this contract are shown on top of a dime in Fig. 2.14 to give a perspective of the dramatic size reduction of microwave components achievable by GaAs monolithic microwave integrated circuit techniques. The second iteration circuit designs require even less chip area while providing improved performance and direct interconnect capability.

2.3 Circuit Design Improvements

The circuit design concepts and fabrication techniques developed for the initial circuit designs were sound and resulted in the functional circuits previously described. However, improvements were necessary to fully comply with the design goals of this program. The improvements described in this section are mostly refinements in the circuit implementation and not changes in the

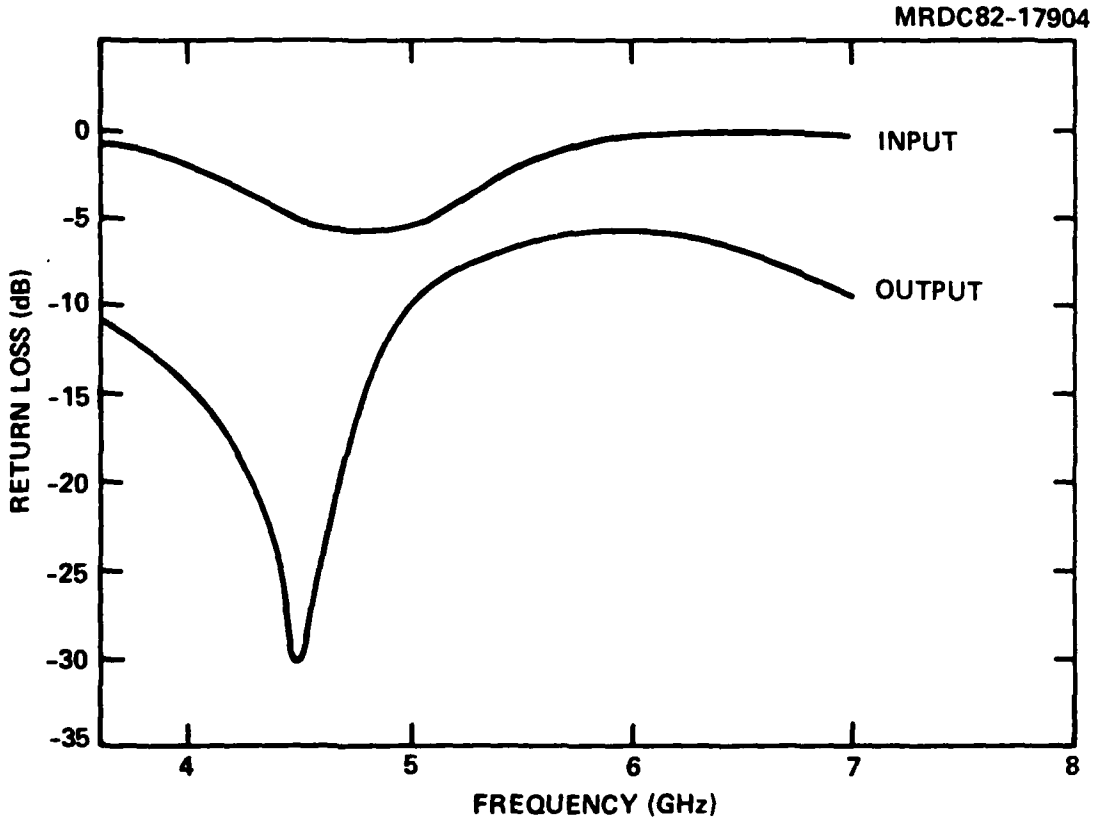

Fig. 2.11 Measured input and output match of the initial 8 GHz preamplifier.

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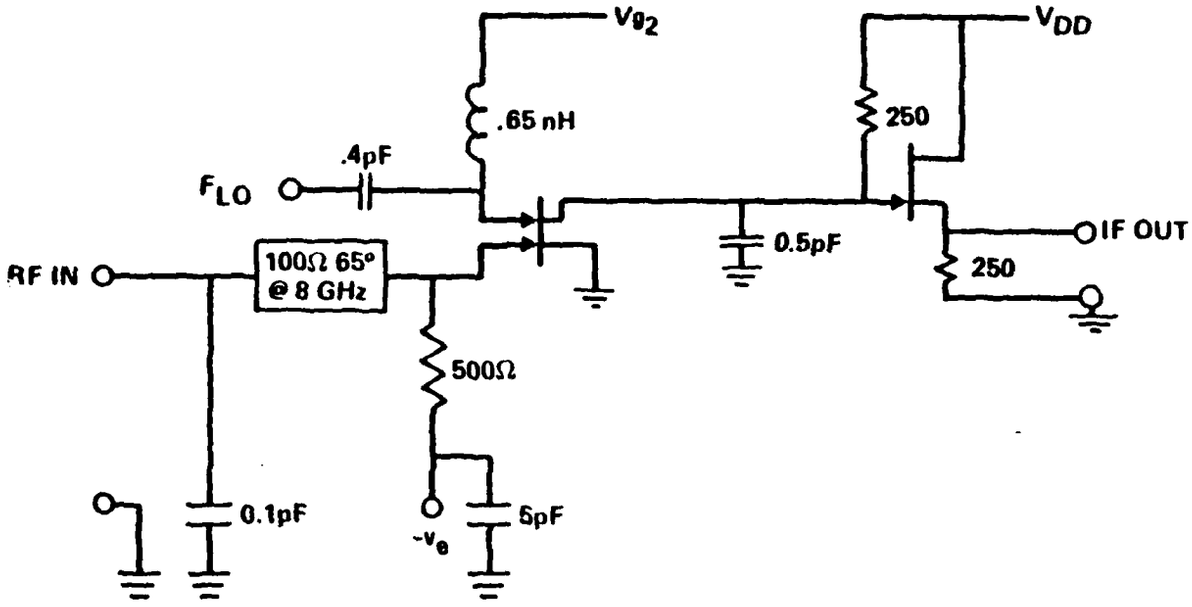

Fig. 2.12 Circuit diagram of the initial 8 GHz dual gate FET mixer.

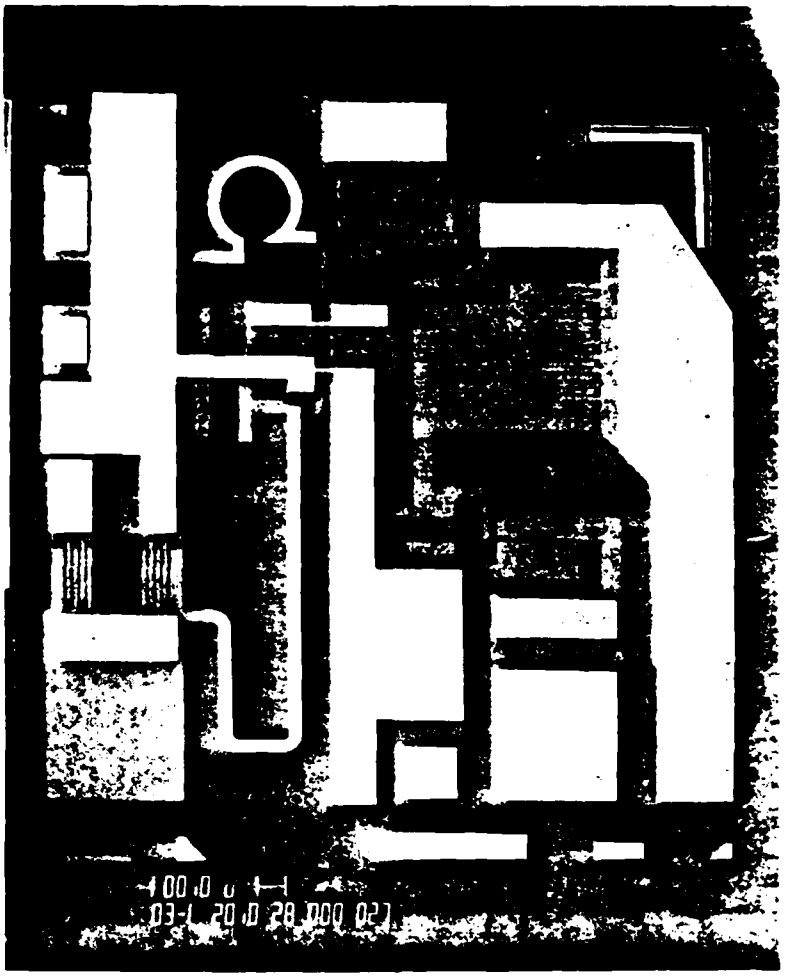

Fig. 2.13 SEM photograph of the initial 8 GHz dual gate FET mixer. Chip size is approximately 2.5 × 2.5 mm^2.

Fig. 2.14 This photograph shows the initial RF preamplifier (left), FET mixer (center), and IF amplifier (right) on the face of a dime. The preamplifier and mixer are each 2.5 × 2.5 mm^2 and the IF amplifier is approximately 2 × 2 mm^2 in size.

basic circuit concepts. Implementation changes centered on improved layout techniques to reduce parasitic elements and improved computer modeling to accurately model those parasitics which could not be eliminated. A local oscillator and a monolithic two-stage preamplifier were included in the second iteration mask set. Evolutionary changes in the processing sequence were continually included as their benefits were verified. These improvements are described in Section 3.0.

As alluded to in the previous section, the major parasitic elements in the first intermediate frequency amplifier design were the "footprint" capacitance to ground of the interdigitated blocking capacitor, and the feedback capacitance between the input and output blocking capacitors. Figure 2.5 showed the predicted gain including these parasitic capacitances, while Fig. 2.3 shows the predicted gain without them. Excellent agreement with the measured data shown in Fig. 2.5 indicates that they are the major performance degrading elements. At one gigahertz parasitic inductive effects on a chip this small are insignificant.

Once the dominant parasitic elements were identified, a new layout was generated to minimize their effect. The schematic remains the same as Fig. 2.1 except that the input bias resistor was increased to 10K and the output source resistor was increased to 250 ohms. The input match is therefore degraded while the noise performance is improved. The change in the output bias resistor merely reflects a lower operating current in the output stage.

The major change in the new chip (shown in Fig. 2.15) is the use of a metal-insulator-metal capacitor in place of the interdigitated capacitor used in the initial design. The "footprint" capacitance to ground is therefore significantly reduced even though the chip thickness was reduced from 635 microns to 250 microns to minimize parasitics in the 8 GHz components on the same wafer. Distance between input and output is maximized to keep feedback capacitance at a minimum, and the thinner substrate further reduces feedback effects. Performance of the new intermediate frequency amplifier is described in Section 4.0.

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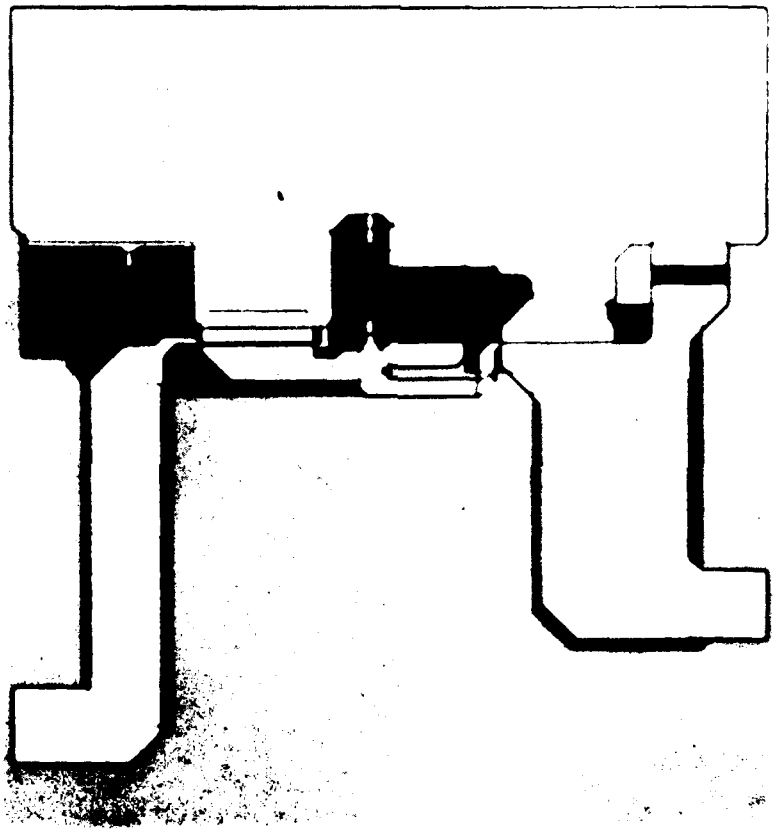

Fig. 2.15 SEM of the improved IF amplifier.

Analysis of the measured data for the initial 8 GHz preamplifier design indicated that several parasitic effects needed correction. Most significant was the conclusion that all inductors must be modeled as distributed transmission line elements to correctly account for capacitance to ground and phase shift due to line length. Additional parasitic capacitances and transmission line losses then accounted for the rest of the discrepancy between predicted and measured results for the first iteration preamplifier chip. Evaluation of the cumulative effect of these parasitic elements on predicted performance is shown in Fig. 2.16. The second generation design employs several techniques to eliminate as many parasitics as possible and to accurately account for the rest.

Substrate thickness was reduced from 635 microns to 250 microns in order to minimize interelement coupling and reduce overall chip size. Distributed transmission line effects are eliminated as parasitics by designing distributed element matching networks from the start. They are then an integral part of the chip design instead of parasitic effects. Chip layout provides a well defined ground plane for source grounding. However, the basic matching network topology remains unchanged with the exception of a small amount of source inductance intentionally included in an attempt to bring the gain and noise match conditions closer together. Figure 2.17 is a schematic of the revised single stage pre-amplifier. Predicted gain and noise figure for this amplifer are shown in Fig. 2.18. Measured results agree well with this predicted data as described in Section 4.0. A photograph of the improved 2 millimeter square single stage preamplifier is shown in Fig. 2.19.

In addition to the single stage preamplifier, a two stage preamplifier with on chip interstage matching and additional on chip bias resistors was designed on a 2 millimeter square chip. Input and output matching networks similar to the one stage preamplifier provide nearly identical noise and VSWR performance.

The input matching circuitry consists of a small series tuning capacitor, which also provides dc blocking for the RF input line, and a shorted stub with associated bypass capacitor for tuning and convenient gate bias

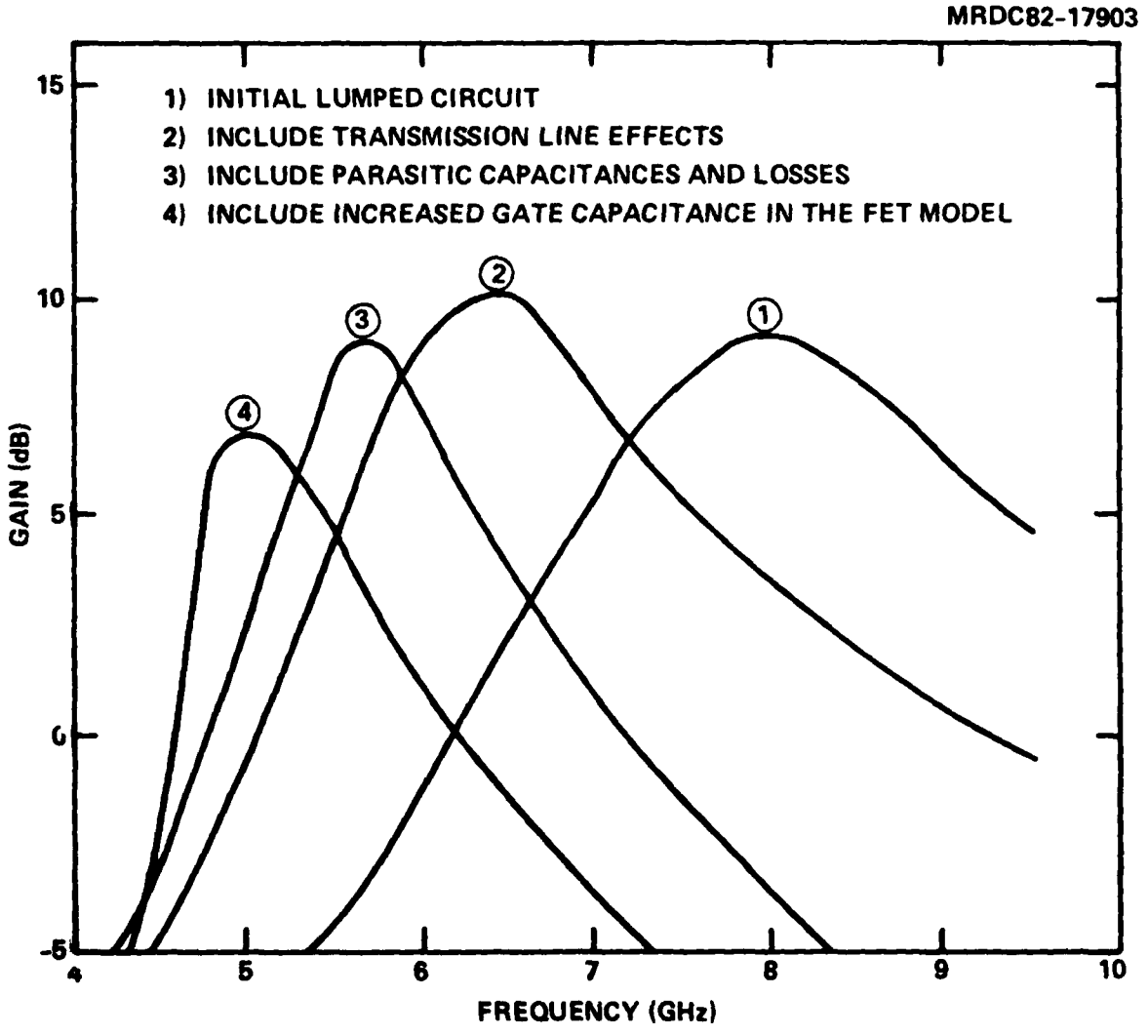

Fig. 2.16 Effect of parasitic on preamplifier performance.

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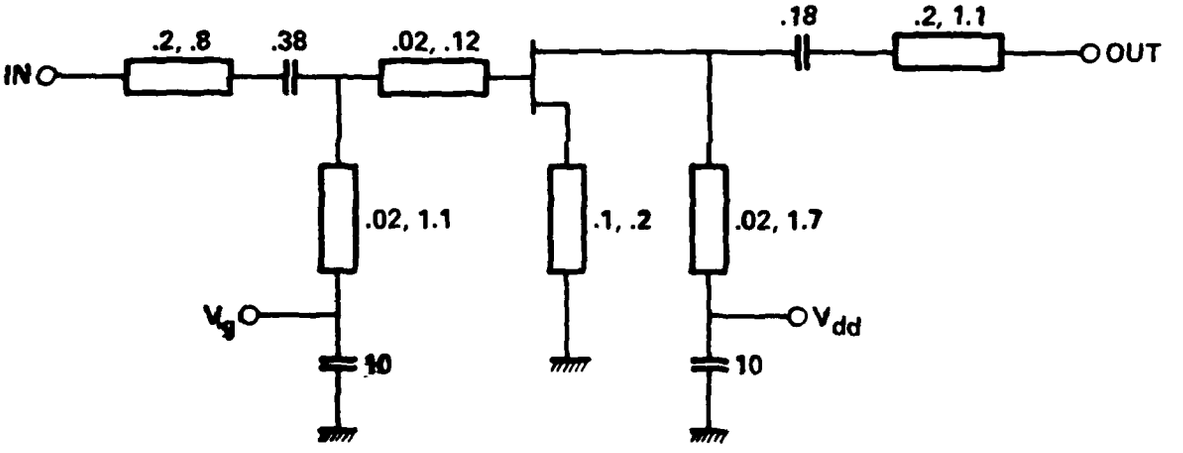

Fig. 2.17 Improved 8 GHz amplifier schematic.

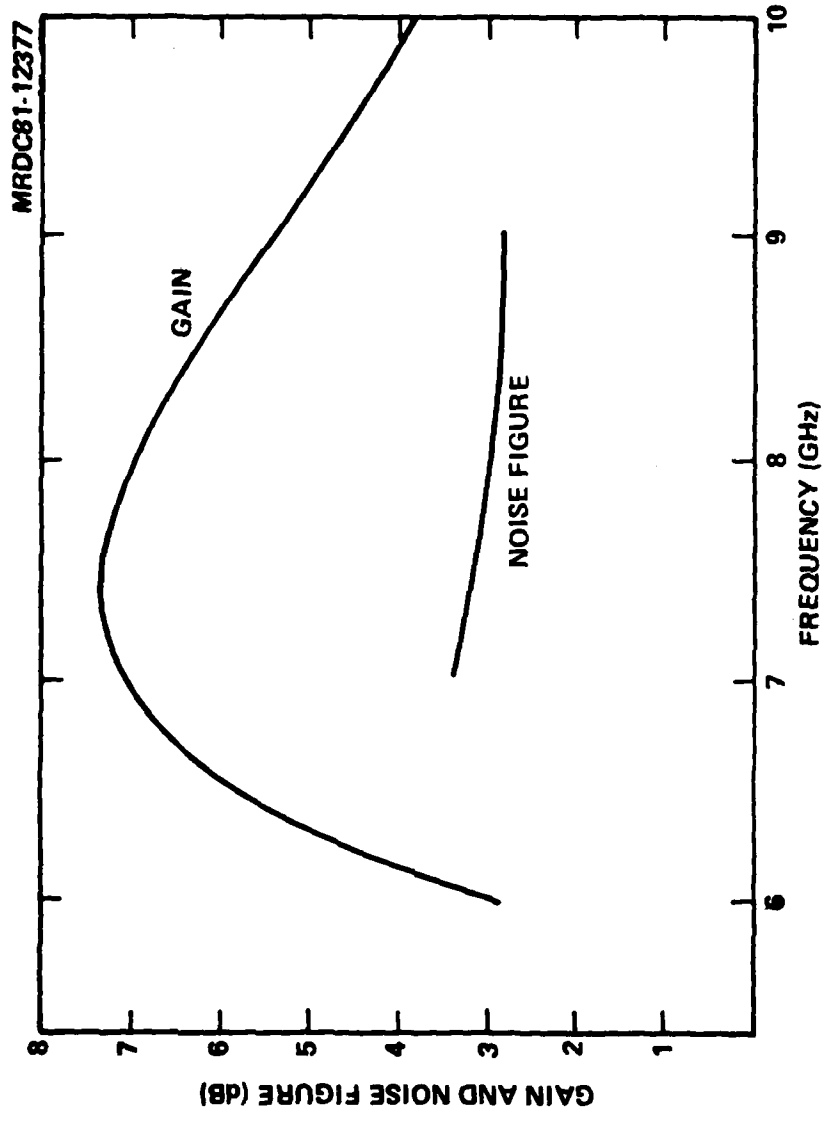

Fig. 2.18 Predicted gain of improved single stage preamplifier.

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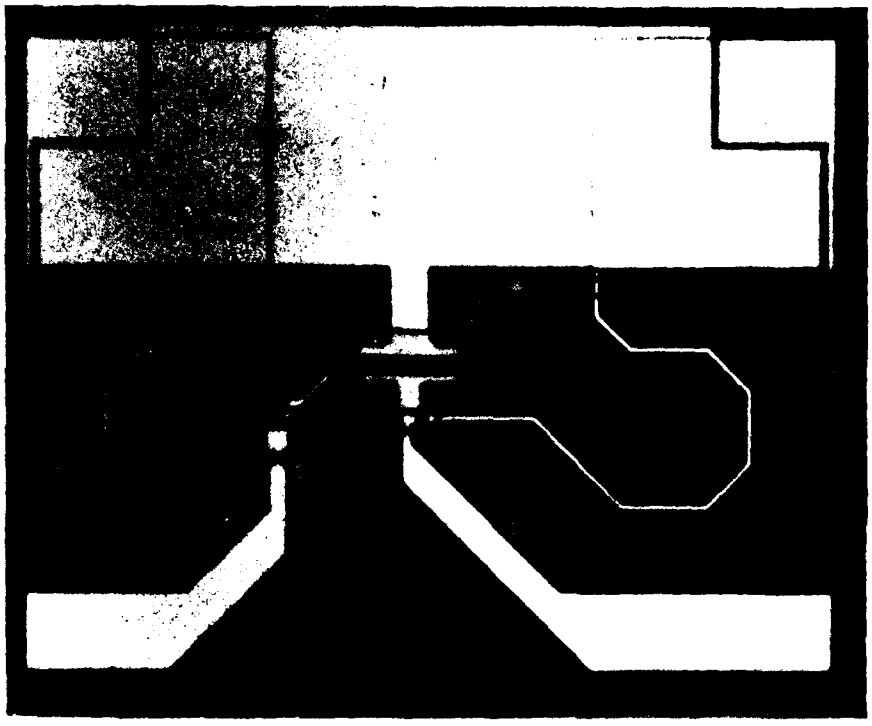

Fig. 2.19 SEM photograph of improved single stage preamplifier.

insertion. A source inductance in the common source FET provides a gain match closer to optimum noise match with only a slight reduction in available gain. Output matching network topology is identical to the input topology, however, the element values are different. The interstage tuning consists of a shunt line for tuning and bias insertion in addition to a series gate inductance. Only two bias lines are needed to power the chip. Figure 2.20 is a schematic of the two stage preamplifier and Fig. 2.21 is a photograph of the chip.

The inherent non-linear nature of mixers and the complex parasitic elements associated with the initial mixer design precluded accurate modeling of the measured mixer results. As an alternative to detailed analysis and modification of the existing design, it was determined that a simple dual gate mixer design capable of a variety of operating modes be fabricated for evaluation. The mixer design selected is based on a novel technique for intermediate frequency extraction first developed under ERADCOM Contract DAAB07-78-C-2999. Figure 2.22 is a schematic of the new 8 GHz mixer circuit and Fig. 2.23 is a photograph of the 2 millimeter square chip. The signal and local oscillator inputs of the mixer are matched in the 8 GHz band by simple lumped/distributed low pass circuitry. The FET associated with the LO input is wider than that associated with the small signal RF input. Complete switching of the RF FET between the triode and pentode regions of operation is assured by this geometry. The IF output is taken between the juncture of the two FETs and is isolated from the 8 GHz signals by a quarter wavelength long section of high impedance transmission line. At the output end of the IF connection, the high impedance line is bypassed to ground through an MIM bypass capacitor. This bypass capacitor is designed to transform to a very high impedance at the FET side of the IF connection thus maintaining a high impedance at this point as required for mixer operation. At the IF frequency, the output transmission line and bypass capacitor form a matching network to provide a good output match to the IF amplifier.

Several operational modes may be implemented with this mixer layout including the following:

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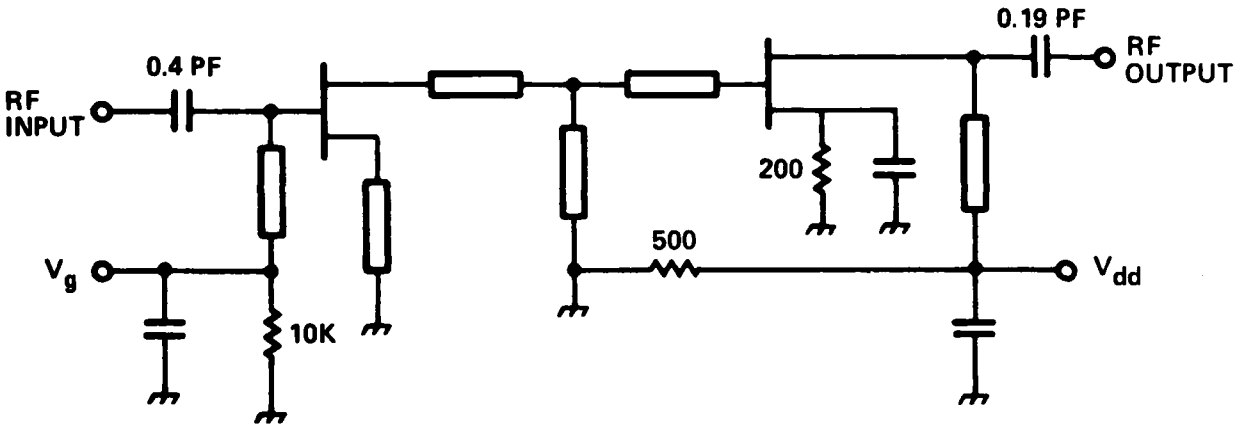

Fig. 2.20 Schematic of two stage preamplifier.

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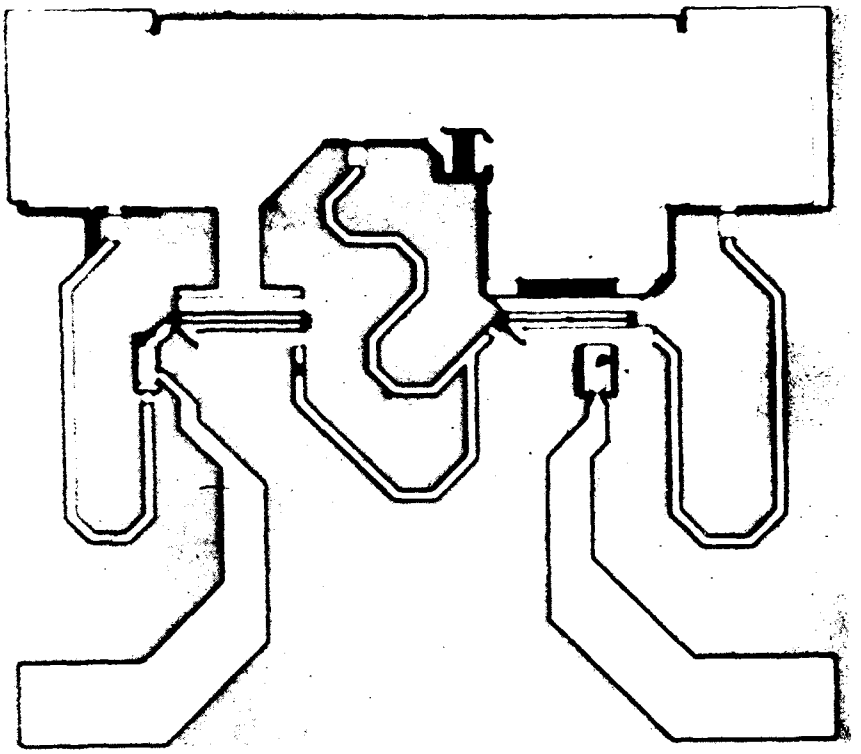

Fig. 2.21 SEM photograph of two stage preamplifier.

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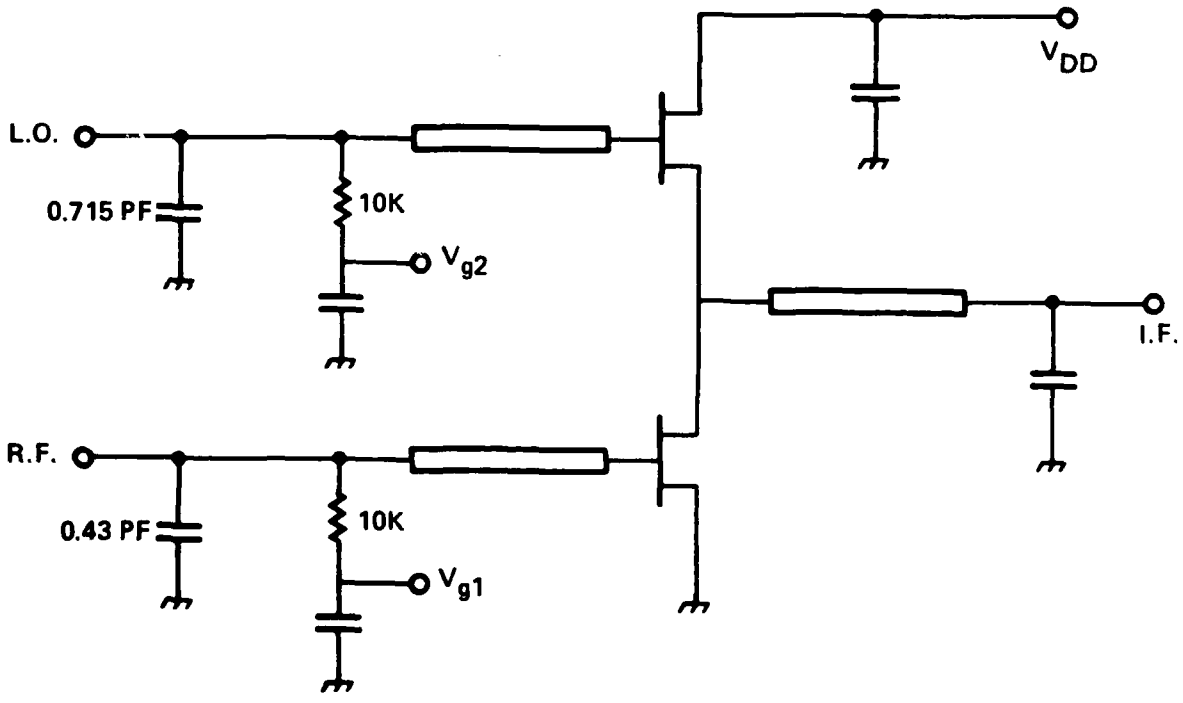

Fig. 2.22 Schematic of improved 8 GHz mixer.

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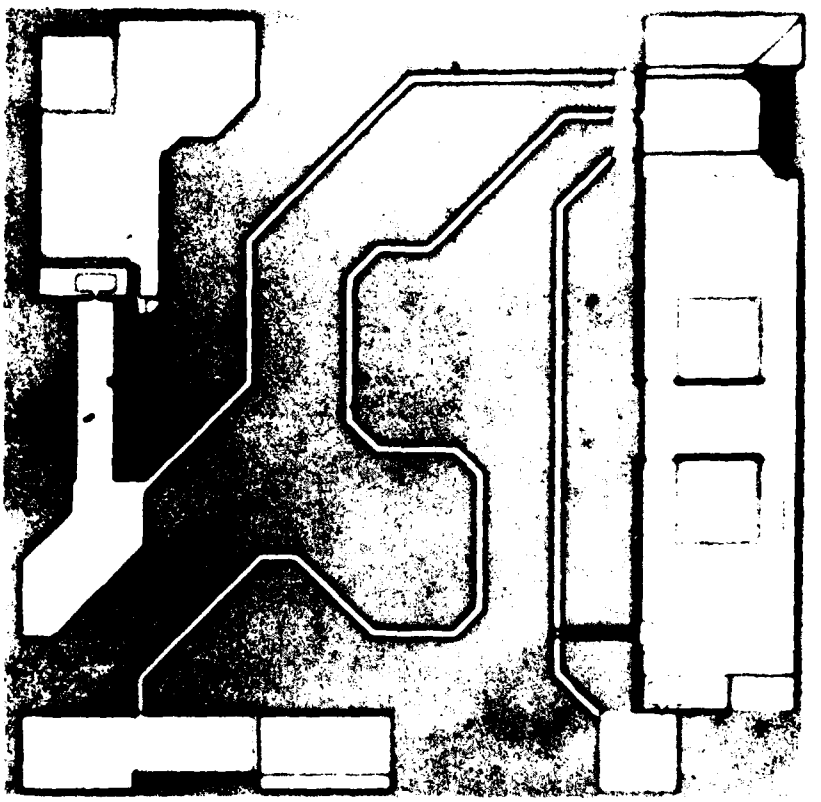

Fig. 2.23 SEM photograph of improved 8 GHz mixer.

Mode	Signal	LO	IF
1	FET 1	FET 2	FET 1 drain
2	FET 2	FET 1	FET 1 drain
	Differential Mode - V_{dd} Applied at IF Connection		
3	FET 1	FET 2	FETs 1 and 2 shared drain
	Dual Gate Mode A		
4	FET 1	FET 2	FET 2 drain
	Dual Gate Mode B		
5	FET 2	FET 1	FET 2 drain

Mode 1 is the primary mode of operation. In this mode of operation, the input impedance of the LO FET will be high due to the source follower configuration, so that appreciable LO drive voltage will be required to properly switch FET 1. The RF FET, which is operating in the common source mode, will be switched between two drain bias states. One bias state is in the triode region and the other is in the pentode region. The high gain state of the mixer occurs when FET 1 is in the pentode state. Due to the complex nature of the interaction which occurs between the two FETs during mixer operation, more detailed analysis requires the assistance of large-signal computer modeling.

The monolithic voltage tuned oscillator was also incorporated on the second iteration mask set. It contains a varactor tuned common-drain oscillator, a common-source buffer amplifier for gain and load isolation, and an active output coupler which provides a sample output to facilitate phase locked operation.

Selection of an oscillator circuit design approach and the design of on-chip peripheral circuits is governed by the need for a compact layout. Whenever possible, large passive structures are replaced by either active

devices or equivalent but smaller passive configurations. Based on these considerations, a varactor-tuned common-drain FET oscillator with a one-stage, common-source, buffer amplifier was selected. Due to the small physical size of the oscillator and the low Q of the elements available on-chip, an off-chip stabilization technique is required. Toward this end, the oscillator is voltage tunable via varactor diodes in the resonator circuit, and an isolated sample of the RF output signal is provided. An active device is used for the sampling function to conserve space. The oscillator chip designed along these lines can then be tested in a variety of configurations. For example, several phase-locked oscillator configurations can be created by the addition of an external mixer(s), a loop amplifier, a filter, and possibly a frequency prescaler. Provision is also made for the direct connection of a high Q external passive resonator.

Figure 2.24 is a schematic of the voltage tuned oscillator schematic including RF and dc bias circuitry. Unique aspects of the design include an active coupler for output sampling and a variable inductance tuning element. A variable inductance is obtained from the parallel connection of a shorted stub and a varactor diode operating below resonance. Tuning the varactor from the smallest possible capacitance to parallel resonance provides an inductance which varies from the inductance of the stub alone up to infinite inductance at resonance. C_{gs} can also be adjusted by varying the gate to source voltage of the oscillator FET thereby fine tuning the oscillation frequency. A photograph of the oscillator chip is shown in Fig. 2.25.

The individual second iteration circuits are designed to allow direct interconnection. All appropriate input and output lines are adjacent in the reticle for simple ribbon bond interconnection to facilitate testing as a receiver front end. Figure 2.26 shows the reticle layout with all necessary interconnections identified. Note that all bias lines are accessed at the edges of the chip to simplify bonding and minimize parasitic coupling.

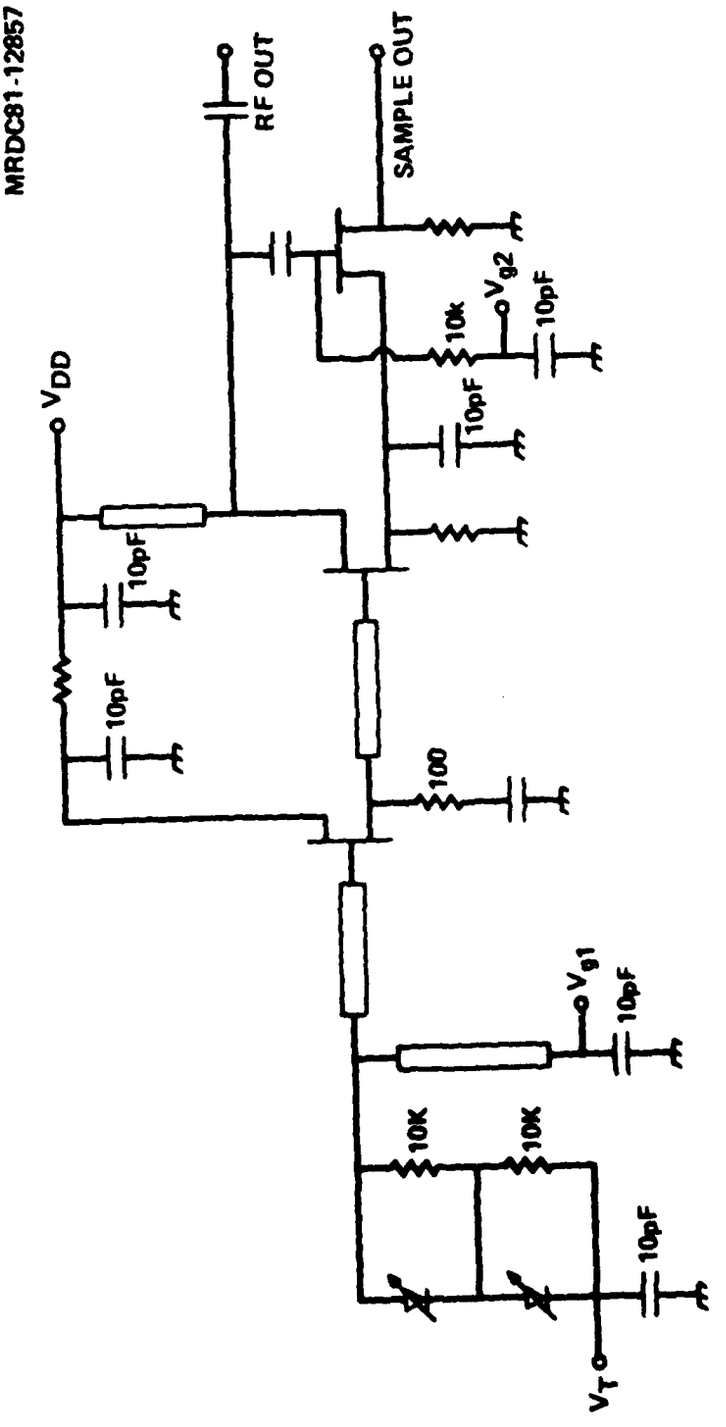

Fig. 2.24 Voltage controlled oscillator schematic.

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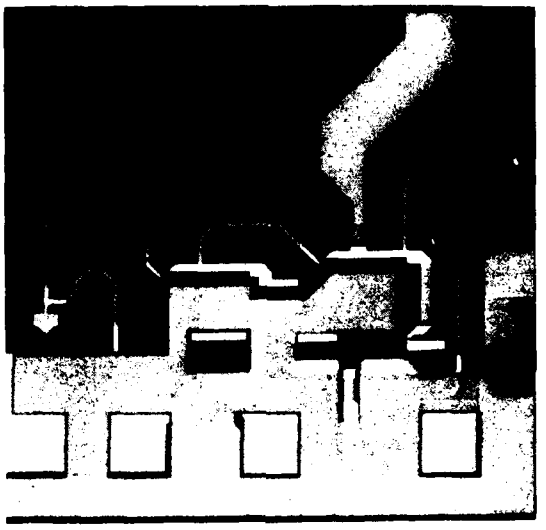

Fig. 2.25 SEM photograph of the oscillator chip.

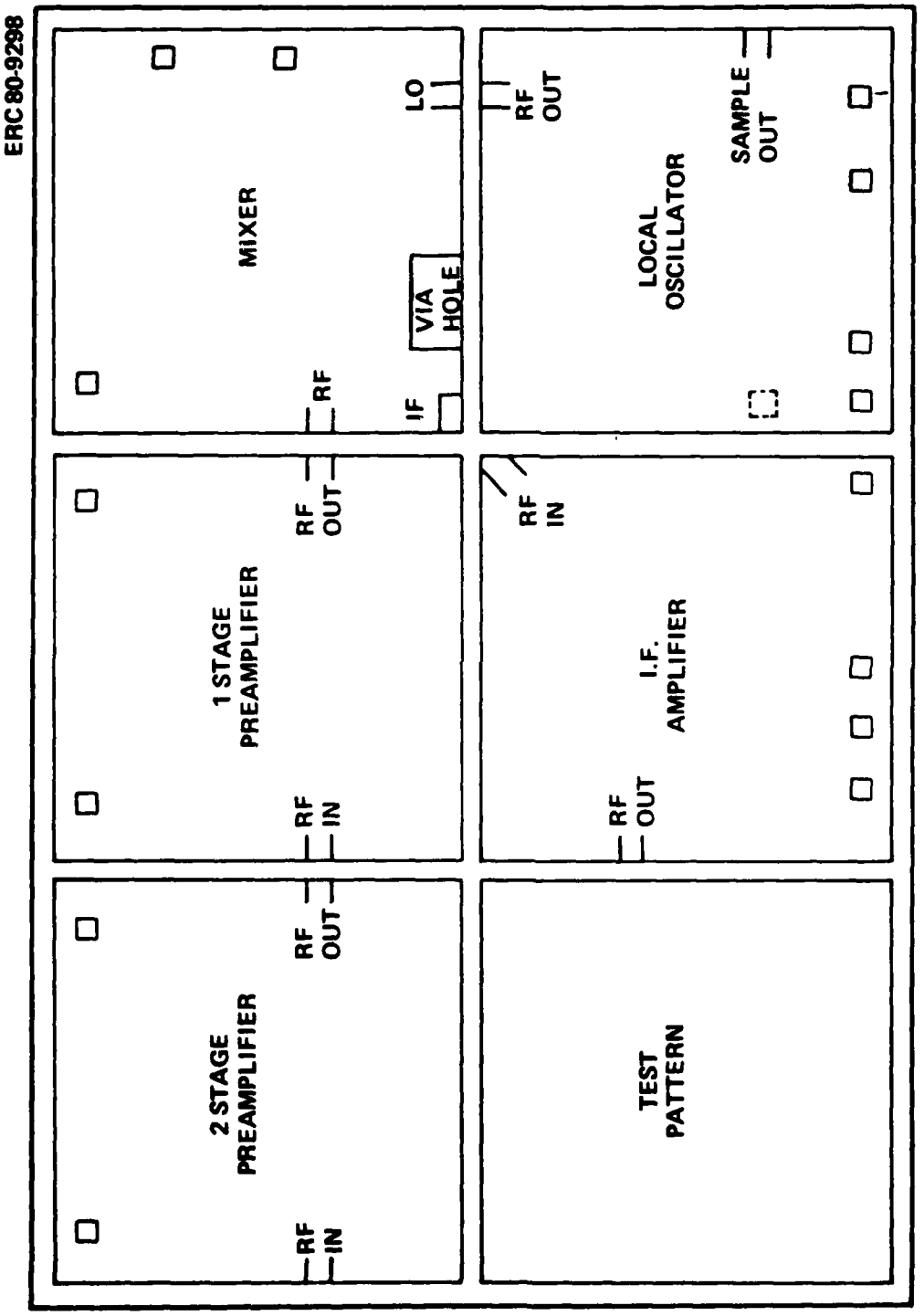

Fig. 2.26 Reticle layout.

2.4 Analysis and Design for Low Noise

The design of monolithic amplifiers for low noise must take into consideration active device properties as well as losses in matching networks and transmission lines to determine optimum noise tuning and achievable noise figure and gain performance. Design of a low noise amplifier thus begins with an analysis of the GaAs FET noise properties and noise parameters to be used in the circuit design. Either theoretical or experimental techniques may be used to arrive at the FET noise parameters. Agreement between the theoretical and experimental numbers obviously instills confidence in the analysis upon which the circuit design is based.

Two approaches have been taken to determining the FET noise parameters for the 8 GHz preamplifier design. In the initial approach, an equivalent circuit model of the FET was synthesized from measured and physically estimated element values for g_m, C_{gs}, R_s, R_g, l_g, etc. This equivalent circuit model was then further analyzed to determine the four noise parameters F_{min}, R_n, G_{opt}, and B_{opt} by including all thermal noise sources such as those associated with R_s and R_g (assumed to be at room temperature) plus the intrinsic FET channel noise at an elevated electron temperature as analyzed by Baechtold. These initial calculated values were used in the amplifier design process to establish constant noise figure circles and an optimum noise match locus for the amplifier.

Thus the amplifier design which was actually fabricated in monolithic form was based on the above noise analysis.

Subsequent to fabrication and testing of the 8 GHz single stage and 2-stage low noise preamplifiers, an extensive noise analysis and design evaluation was performed using the Fukui approach. This approach is based on thorough dc characterization of the GaAs FETs to obtain device parameters which are inserted into a simplified FET noise model which is based on the Pucel noise theory. Thus, the Fukui approach combines both theoretical and experimental elements to yield estimates of the FET noise parameters which are based on actual dc measurements of device characteristics. This approch can be a very powerful tool

for analyzing the relative significance of noise contributions due to the intrinsic FET noise, deviations from optimum noise match, and circuit losses.

The initial noise model used for amplifier design was based on the equivalent circuit shown in Fig. 2.27 with the element values given below in Table 2.4-1A. The calculated FET noise parameters using the initial analytical approach (hot electron model) are given in Table 2.4-1B. A Fukui analysis of the FET model given in Table 2.4-1A was done after the amplifiers were fabricated and gave the noise parameters shown in Table 2.4-1C. Based on these new estimates of F_{min} and measured data from similar discrete FETs on the same mask set, it was decided to evaluate a recessed gate structure for the FET. Table 2.4-1D is a summary of the relevant noise parameters for the recessed gate FET, which now attains the desired RF performance. In fact, actual measured performance of the single stage amplifier with a recessed gate FET indicates that this Fukui analysis is somewhat pessimistic (see Section 4 for further measurement results).

Scrutinization of Table 2.4-1 reveals several features about the various noise analysis techniques. Although F_{min} for the hot electron model appears overly optimistic, the large R_n indicates an increased sensitivity to tuning variations which tends to offset the optimistic noise figure estimate. The optimum noise match predicted by the two models are also substantially different. The real part of Y_{opt} is in good agreement, however, the imaginary part differs by a factor of four. However, it is important to note that Y_{opt} is almost constant as the gate is recessed according to the Fukui model, while F_{min} is reduced. This means that an existing amplifier layout will provide improved performance as the gate is recessed, without the need for revised tuning. Experimental results tend to verify this observation.

More analytical work is required to obtain good correlation between theoretical noise models and measured performance. In the meantime, a combination of measured data and empirical formula with a basis in theory (such as the Fukui technique) can lead to sufficient information for low noise monolithic circuit design. Accurate characterization of discrete FETs is crucial if optimum noise performance is desired.

Table 2.4-1

Initial FET Noise Analysis

A: Salient FET Parameters (Assumed)

C_{gs} = 0.2 pF g_m = 18 mS

R_g = 5 Ω R_i = 2 Ω R_s = 2.5 Ω

B: Noise Parameters from Hot Electron Model

f (GHz)	F_{min} (dB)	R_n (X)	G_o (mS)	B_o (mS)
7	2.20	79.6	9.07	-2.42
8	2.48	78.3	10.42	-2.77
9	2.75	74.9	11.75	-3.05

C: Noise Parameters from Fukui Model

C_{gso} = 0.5 pF g_{mo} = 24 mS

7	1.63	44.4	3.08	-7.47
8	1.83	44.4	3.85	-8.18
9	2.01	44.4	4.65	-8.78

D: Noise Parameters for Fukui Model (Recessed Gate)

7	2.72	29.63	10.5	-13.9
8	3.00	29.63	12.4	-14.3
9	3.26	29.63	14.1	-14.4

3.0 CIRCUIT FABRICATION TECHNOLOGY

The circuits described in this report have been fabricated on semi-insulating gallium arsenide (GaAs) substrates using high-yield, state-of-the-art processes. Complex monolithic microwave integrated circuits (MMICs) require more than one type of device (FETs, Schottky diodes, bulk resistors, etc.) for their operation and the optimization of the performance of each device may require more than one type of active layer on the same substrate. To accommodate this need, the fabrication techniques implemented in this program are based on multiple, localized ion-implanted active layers which makes it possible to define fabrication processes not possible under the limitations of epitaxial growth or implantation over the full wafer. The uniformity, reproducibility, versatility, and low cost of ion implantation technology are difficult to match by other materials technologies. Due to the faster turnaround possible with implantation over the whole wafer in conjunction with mesa etching, this approach was taken when only one type of active layer was required.

A schematic diagram of an MMIC is shown in Fig. 3.1. The circuit is fabricated on a semi-insulating GaAs substrate which provides dc isolation and low parasitic coupling between various active devices and circuit elements. Typical components required are capacitors, resistors, transmission lines, FETs, varactor diodes, and level-shifting diodes. In addition, it is necessary to provide ground points, dc bias points and RF connections. A two-level metallization scheme is used with plasma-deposited silicon nitride as the crossover insulator and the dielectric for metal-insulator-metal capacitors. Capacitors can be either interdigital or metal-insulator-metal depending on the application. MIM capacitors have been used exclusively in the second generation receiver circuits because interdigital capacitors of the required value consume a large chip area and have unacceptable high parasitic capacitance to ground. Good control on the yield and value of MIM capacitors has allowed their use for RF tuning as well as bypassing. Capacitance per unit area of approximately 130 pF/mm^2 or higher is presently attainable with this technology. Resistors are fabricated either by ion implantation or thin film deposition. Thin film

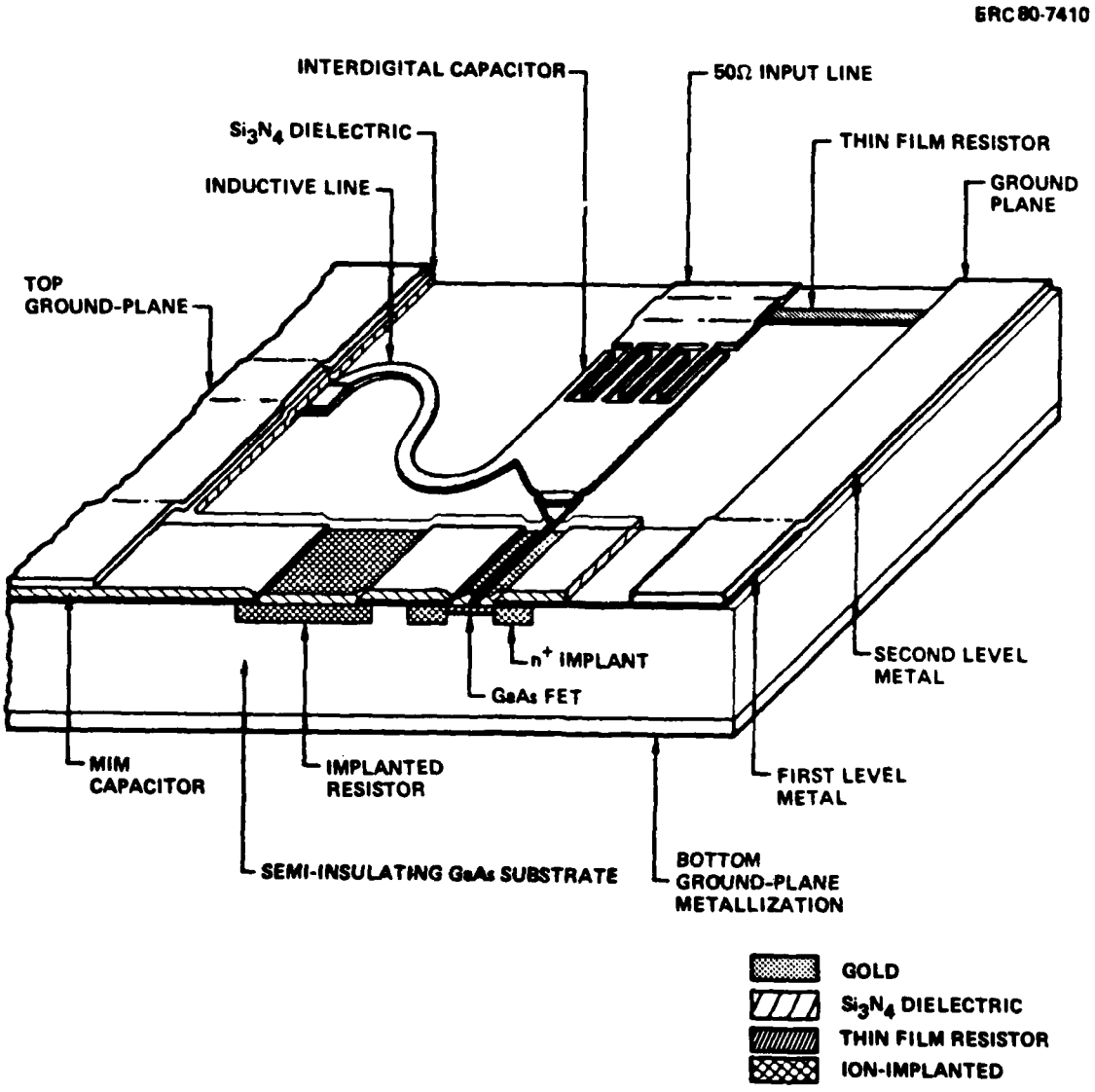

Fig. 3.1 Schematic diagram of a monolithic microwave integrated circuit.

resistors have a larger linear region but require an additional mask level. Self-biased FETs or saturated ion-implanted resistors can be used for large values of incremental resistance, e.g., current sources.

Transmission lines are constructed in the form of micro-strip. Co-planar and slot line techniques consume large chip areas and can cause interconnection problems. RF interfaces are provided as 50-ohm transmission lines that run to the edge of the chip. DC connections are made to bonding pads with their associated metal-insulator-metal bypass capacitors.

Fabrication of the structure described above requires highly sophisticated technologies. Both substrate selection and the fabrication process must be carefully controlled. These topics are discussed in greater detail in the following sections.

3.1 GaAs Materials and Ion Implantation Technology

3.1.1 Semi-Insulating Substrate

Previous lack of control in the preparation of semi-insulating GaAs substrates has led to the development of qualification procedures which assess the suitability of individual ingots for direct ion-implantation processing. Typically, ingots are doped with chromium to compensate the background impurities and insufficient control in crystal growth can result in thermal conversion of the semi-insulating substrates under certain circumstances. High levels of chromium can also degrade the mobility and crystalline quality of these materials and cause significant impurity redistribution during thermal cycling. In view of these considerations, the following conditions must be met to allow the successful implantation of an active layer:

1. The compensating impurities and defects in the substrate must not affect the electrical properties of the ion-implanted layer, so that carrier concentration, mobility, carrier lifetimes, etc. depend only on the identity and dose of the implanted ions. Meet-

ing this condition ensures that the electrical properties of the implanted layers are independent of the substrate, and guarantees that implanted layers can be prepared reproducibly.

2. Unimplanted portions of the semi-insulating substrate must retain high resistivity after a wafer has been capped and annealed so that electrical isolation is maintained between the doped regions.

3. The substrate must be homogeneous. This implies that conditions 1 and 2 must be met with a minimum of short and long-range inhomogeneities or defects. In addition to homogeneity, exacting wafer flatness control must be maintained to achieve high yield for small geometry devices.

Two major types of commercially available semi-insulating GaAs substrates have been used for MMIC fabrication, as outlined below:

a. Chromium doped semi-insulating GaAs grown by horizontal Bridgman or gradient freeze methods.

b. Undoped and chromium doped semi-insulating GaAs grown by the Liquid Encapsulated Czochralski (LEC) techniques.

Qualification Tests for Ion Implantation

The preselection tests for bulk semi-insulating substrates involves qualification of the entire GaAs ingot by sampling wafers from the front and rear of each boule. Extensive data has shown that all wafers within the ingot will be acceptable when samples from both ends of the boule pass the qualification tests. The electrical criterion for qualification involve the following two tests:

1. Thermal Stability: The semi-insulating GaAs samples are capped with 1100Å sputtered Si_3N_4 and annealed at 850°C for 30 minutes in a H_2 ambient. After removal of the Si_3N_4 cap, Au-Ge-Pt ohmic contacts are formed and the sheet resistance is measured. A sheet resistance > 10^7 ohms/square is required to pass this test. The uniformity of sheet resistance across the wafer and variation between the two ends should be within 10 percent. This test provides assurance against thermal conversion of conduction type and gross resistivity degradation effects.

2. Ion Implantation Test: A 3.0×10^{12} cm^{-2}, 125 KeV silicon ion implant is performed at room temperature. Samples are then capped and annealed as in (1). Following annealing, the cap is stripped and aluminum Schottky barrier metal is evaporated onto the test samples. Doping profile and mobility measurements are made to characterize the active layer and verify that it is suitable for device fabrication. Activation > 80 percent, electron mobility > 4500 cm^2/Vsec and a peak carrier concentration of ~ 1.5×10^{17} cm^{-3} with depth at a concentration of 10^{16} cm^{-3} of 2600 ± 300Å is required. The uniformity of doping profile across the wafer and variation between the front and the tail end of ingot is required to be within 5 percent to permit a reproducible implant profile in the active layers from wafer to wafer.

3.1.2 Profile Synthesis and Characterization

Choice of Dopant

The n-type dopants that have been most extensively explored as implantation species in GaAs are listed in Table 3.1-1. The calculated implant energy required to obtain a range of 1000Å is listed along with the corresponding straggling, skewness, and diffusion length resulting from an annealing schedule of 850°C for 30 min. Thus, the listed parameters are representative of typical

FET active layer implants. The require implant energy ranges from 120 KeV for Si to 460 KeV for Te, which is the heaviest element listed. The trend toward negative skewness favors the use of the lighter dopants.

Table 3.1-1

n-Type Implants Into GaAs With a Calculated Range of 1000Å

Dopant	Energy (keV)	Straggling (nm)	Third-Order Moment	Diffusion Length* (nm)
Si 28	120	51	-0.104	60
S 32	140	60	0.7	+
Se 79	300	44	0.293	47
Te 127	460	41	09.60	38

*Annealing condition: 850°C for 30 min.
+Varies greatly depending on cap material.

Si, S, and Se have been used in our laboratory for MMIC active layers with Si as the preferred dopant because of its high activation and excellent profile reproducibility. Si implants can be done at room temperature (instead of 200°C, as required by the other elements) thereby permitting greater sample throughput. Implants are carried out using an Extrion 400 KeV implanter. A 1.4 μm thick photoresist layer is used as an implantation mask when necessary. Typical implantation conditions are as follows:

1. FET and Bulk Resistor Active Layer
   - Ion: ^{29}Si
   - Temp: ~ 23°C (Room Temp)
   - Dose: 3.0 E12 cm^{-2}, 125 KeV

2. n^+ Contacts
   - Ion: ^{29}Si
   - Temp: ~ 23°C (Room Temp)
   - Dose: 1 E13 cm^{-2}, 250 KeV

The FET channel implant has a peak doping of 1.5 - 2.0 × 10^{17} cm^{-3} at a depth of ~ 1000Å below the GaAs surface and yields a sheet resistance of ~ 1000 Ω/□. Both Se and Si have been used as implant species, though Si is preferred as mentioned previously. A typical doping profile is shown in Fig. 3.2. This active layer is suitable for bulk resistors as well as non-recessed-gate FETs and the mask set has been designed to allow implantation of both active layers simultaneously. During the last phase of this program, the implantation schedule was changed to form a more heavily doped active layer. This was used in conjunction with recessed gate technology to improve the noise figure of the device by reducing the gate-source parasitic resistance. Details of the various improvements in FET fabrication for obtaining low noise devices are presented in Section 3.4.

3.2 GaAs MMIC Fabrication Technology

The first generation receiver circuits fabricated in this program had 635 μm thick S.I. GaAs substrates and used microstrip transmission line circuitry. Top surface ground planes were provided near the chip edges to allow low parasitic inductance grounding of active and passive devices. Second generation circuits used a 250 μm thick S.I. GaAs substrate which allowed a more compact chip layout as discussed in Section 2.0. An implant of ~ 1000 Ω/□ was used for FET and resistor active layers. The implant species was Se for the early circuits and Si for the later ones. Contact photolithography was used for all pattern steps including definition of the 1.0 μm long gates. Silicon nitride deposited by plasma enhanced CVD was used as the dielectric in metal-insulator-metal capacitors and as the insulator in a two level metallization process. Excellent uniformity and reproducibility of MIM capacitors has allowed their use for both RF tuning and bypassing. Except resistors, all microwave circuitry was on the second metallization level which was electroplated to a thickness of ~ 2 μm to minimize losses. The mask set had seven levels as described below:

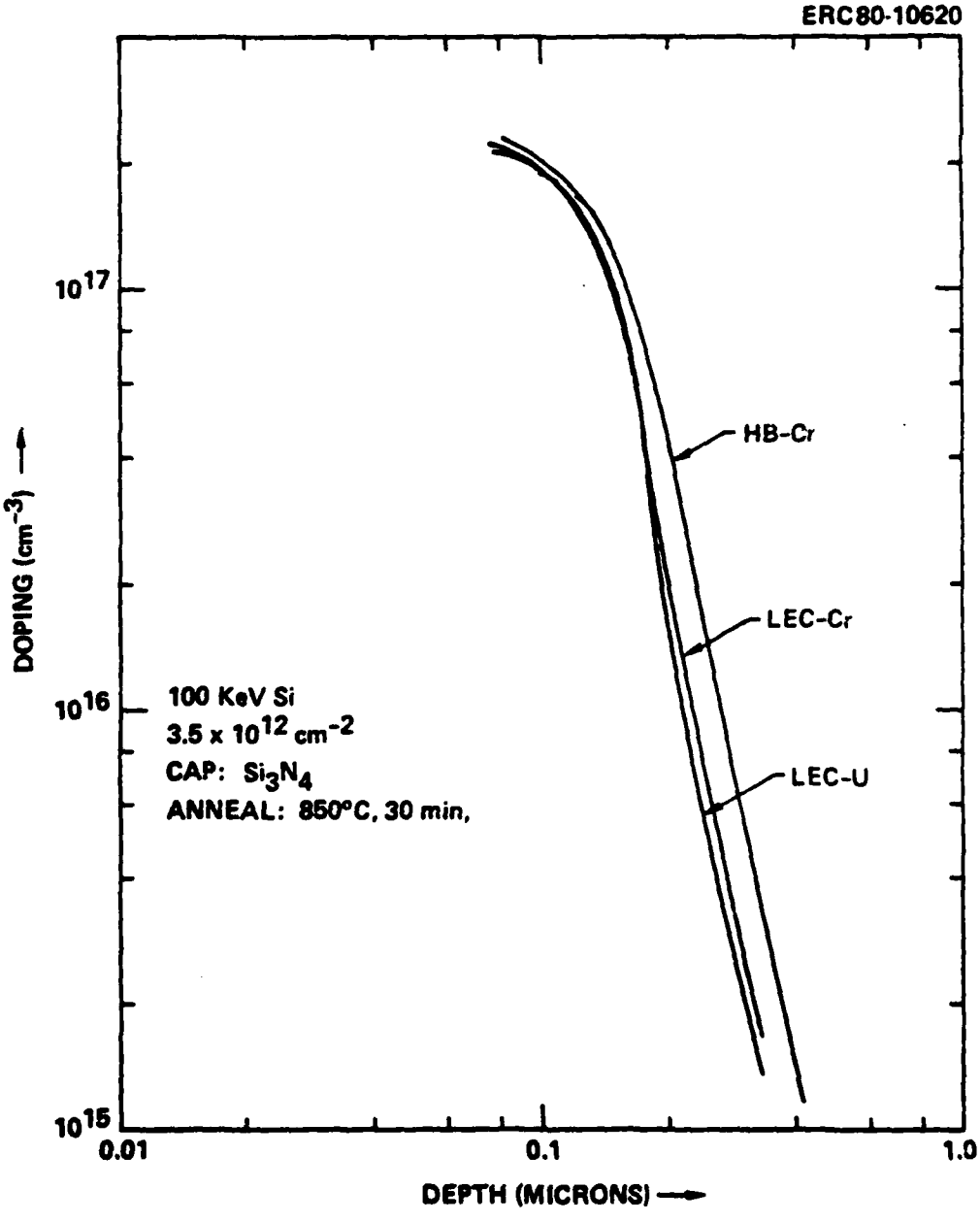

Fig. 3.2 Ion implantation doping profiles in LEC and Bridgman semi-insulating GaAs substrates.

Level	Function
1	Mesa/Active Layer
2	Ohmic Contact
3	Gate and First Level Metal
4	Via Hole (Dielectric)
5	Second Level Metal
6	Fiducial Alignment Marks
7	N^+ Contact

All seven levels are needed if a planar circuit with n^+ contacts is to be fabricated. If however, a mesa approach without n^+ contacts is desired, only the first 5 mask levels need be used. Details of the important fabrication steps are given next.

(1) Active layer implant: Si, 125 keV, 3.5×10^{12} cm^{-2} with substrate at room temperature. A peak doping of $\sim 1.5 \times 10^{17}$ cm^{-3} and a pinch-off voltage of ~3.5 volts is obtained. Definition of active areas may be accomplished by either mesa etching or by selective implantation using a photoresist mask. Fiducial alignment marks are defined on the wafer surface for subsequent realignment capability when localized implantation is used.

(2) Cap and anneal: 1100A of reactively sputtered silicon nitride is used as a cap. Annealing is done at 850°C for 30 min in hydrogen.

(3) Define mesas (as necessary): This step is required only if the implantation is made over the entire wafer. Although this results in a nonplanar structure, it is often used to reduce the turnaround time. 3000A high mesas are defined using a chemical etch.

(4) Form ohmic contacts: Eutectic Composition Au Ge (1000A) and Ni (150 A) are evaporated using an electron beam source. The contacts are alloyed at 450°C for 1 minute in forming gas.

(5) Deposit silicon nitride by plasma enhanced CVD. This nitride layer is used to define the FET gate and the overlay metal as described below.

(6) Deposit Gate and First Level Metal (Ti/Pt/Au): The importance of being able to reliably define the gate electrode of FETs cannot be overemphasized. In order to minimize the parasitic gate resistance, the thickness of the gate metal must be made as large as practical. The yield of the gate definition step, however, decreases rapidly with increasing metal thickness when conventional lifting techniques are used (such as single layer photoresist). In order to improve the lifting capability, the process shown in Fig. 3.3 has been developed. A layer of silicon nitride is deposited on the GaAs and the gate pattern is defined in the photoresist. The exposed nitride is then etched in a CF_4 plasma. Due to the increased distance between the top of the resist and the surface of the GaAs, thicker metallization may be deposited and lifted. Figure 3.4 shows two 1 μm long gates, spaced by ~1 μm, in a 6 μm gap between the source and the drain of a dual gate FET fabricated in this manner. The metallization is 5000A Ti-Pt-Au. Note the excellent edge definition obtained by this technique. Reactive ion etching was used here to minimize the undercutting in the nitride.

The first level metallization contains the bottom plates of MIM capacitors, ohmic contact overlays, and interconnecting lines. In attempting to define these patterns by conventional lifting techniques, it was observed that the edges were ragged due to the

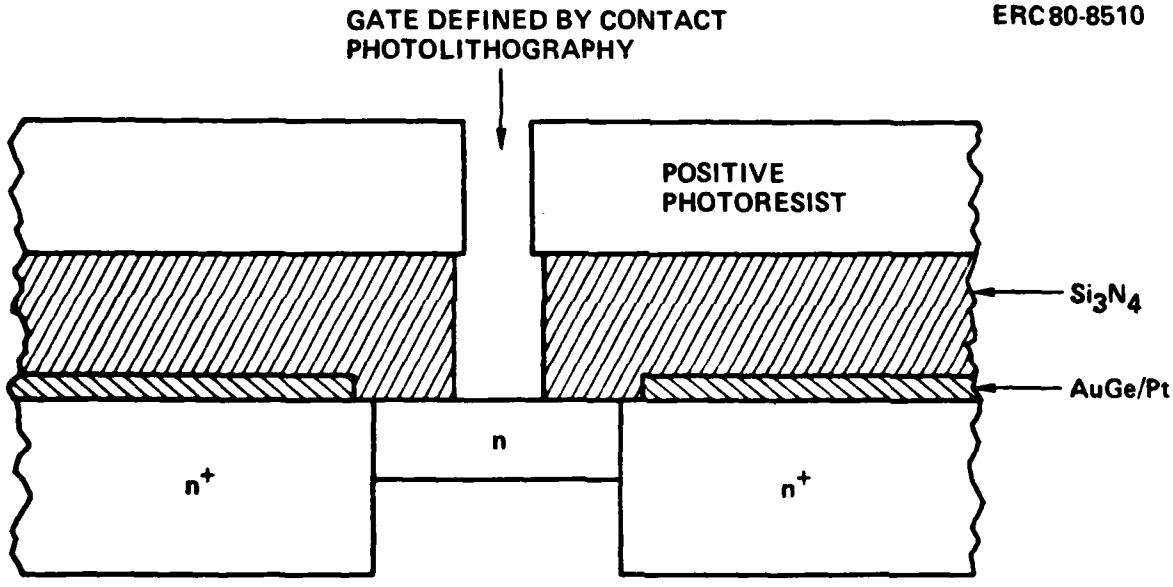

Fig. 3.3 A schematic diagram showing the nitride-aided lifting process. Si_3N_4 deposited on GaAs and the gate pattern is defined in positive photoresist on top. Exposed Si_3N_4 is etched in a plasma. Gate metal is then evaporated and lifted as usual.

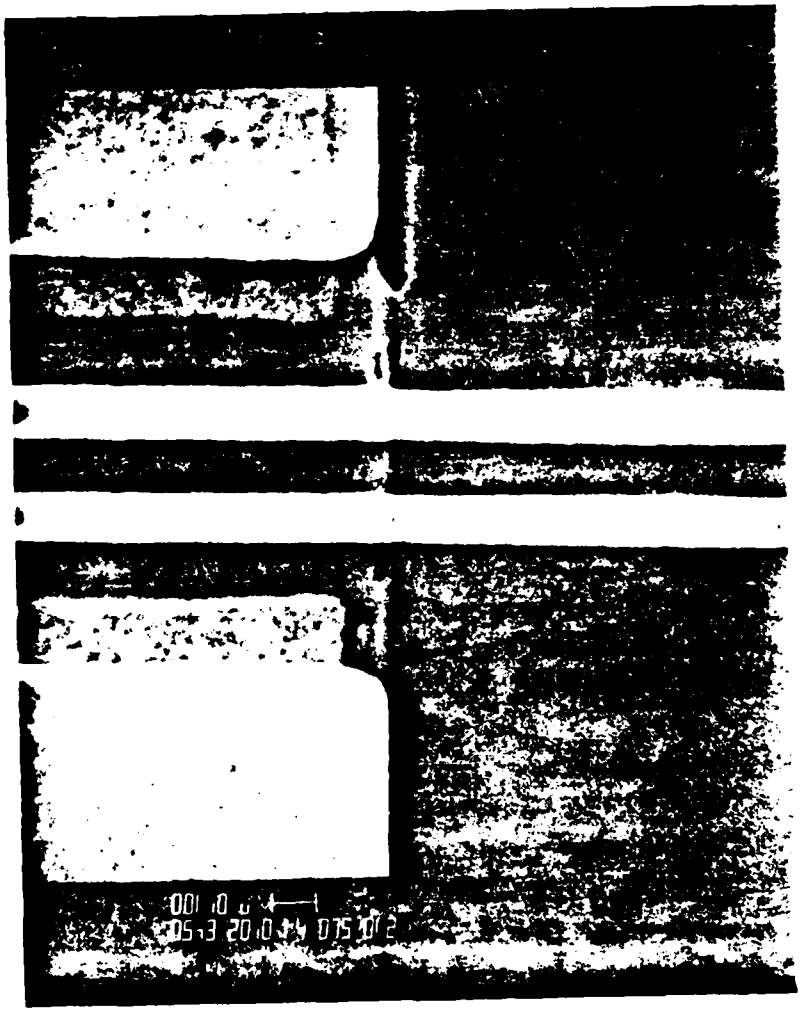

Fig. 3.4 Photograph showing the excellent edge definition obtained with nitride-aided lifting. The two gates (~ 1 μm long) are spaced 1 μm apart in a 6 μm source-drain gap. Metal thickness is 5000Å.

tearing involved at these points. This is shown schematically in Fig. 3.5a. These sharp edges are not well covered by the subsequent step of dielectric deposition which forms the "I" layer of MIM capacitors. This results in a very poor yield of MIM capacitors due to shorts between the first and the second metallization levels along the overlap periphery. The nitride aided lifting process substantially reduces these sharp edges provided metallization thickness is less than the nitride thickness and improves MIM capacitor yield (Fig. 3.5b). This approach was used to fabricate the MMICs described in this report. Further investigation of the MIM capacitor yield problem has revealed that definition of the first metallization level by an etching process rather than by liftoff results in further improvements in yield. Results of this study are summarized in Section 3.3.

(7) Deposit second layer silicon nitride by plasma enhanced CVD. This nitride layer is used as the dielectric for the MIM capacitors and as the insulator for crossovers. It also provides a protection layer for the FETs.

(8) Open via holes: Via holes are opened in the silicon nitride layer wherever connections to the first level metal are desired. Standard photolithography and plasma etching is used for this purpose.

(9) Deposit second level metal: This metallization (Ti/Au) is used for the top electrode of MIM capacitors and all the interdevice matching circuitry. The gold is usually electroplated to a thickness of ~2-3 μm to reduce ohmic losses.

(10) Lap backside to achieve the desired wafer thickness (250 μm).

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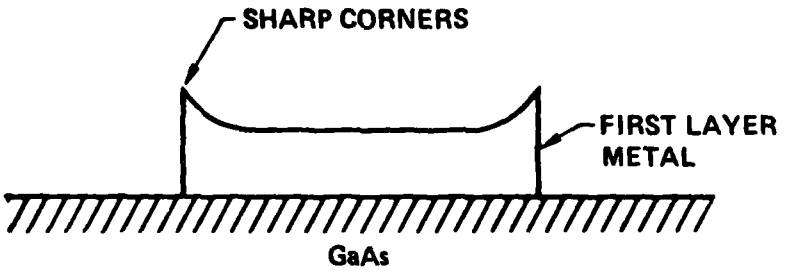
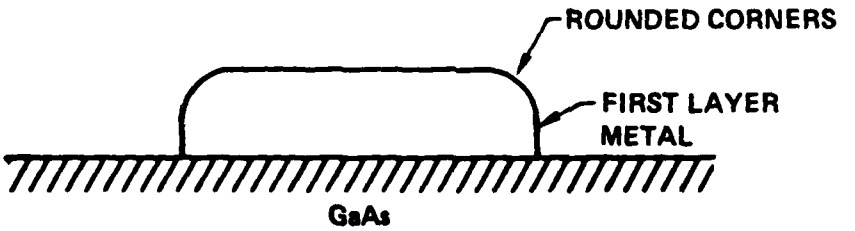


(a)



(b)

Fig. 3.5 (a) Sharp corners obtained in attempting to define thick metal patterns by the lifting technique; (b) rounded corners obtained by chemically etching or ion milling the unwanted metal.

(11) Metallize backside: Pd is first deposited using an electroless process. This is followed by ~ 2 μm of electroplated gold.

(12) Saw wafer into individual chips.

Photographs showing the circuits are given in other sections of this report.

3.3 Yield Considerations

The processing sequence described in the previous section has been extensively used in our laboratory for fabricating MMICs. Yield data on some critical fabrication steps, obtained using the test pattern of Fig. 3.6 is presented in this section. This test pattern has been developed for process monitoring and is present on all our MMIC mask sets.

The uniformity and reproducibility of active layers formed by direct, localized ion implantation in qualified semi-insulating GaAs substrates has been measured. Figure 3.2 shows the reproducibility of a 100 KeV Si implantation profile in different types of substrates processed at different times. Additional data is provided in Table 3.3-1, where the average I_{dss} before gate recess of 200 μm wide FETs is given for various substrates. These wafers were also processed separately and the data shows very good uniformity and reproducibility of implant activation. Data on pinch-off voltage uniformity is shown in Fig. 3.7 and it confirms the excellence of this technique for active layer formation.

Ohmic contacts are formed by sequential evaporation of AuGe and Ni, lift-off, and alloying at 450°C. This metallization scheme consistently results in low resistance contacts as shown by the data in Table 3.3-2. This data was obtained on randomly selected wafers at the completion of front-end processing and shows that it is possible to maintain a low specific contact resistance ($\sim 1 \times 10^{-6}$ ohm cm^2) through the 250°C silicon nitride deposition steps.

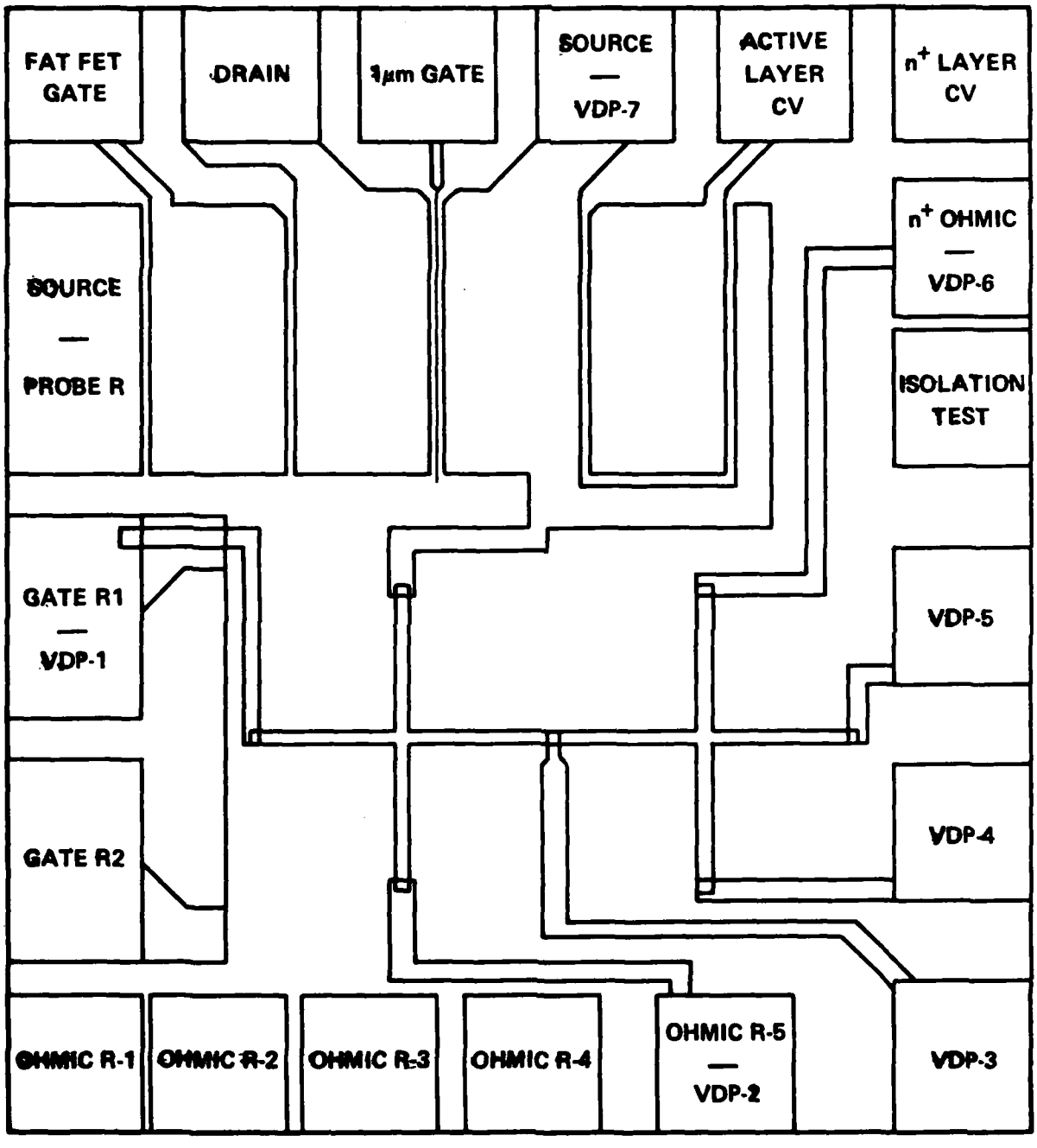


Fig. 3.6 Process evaluation chip.

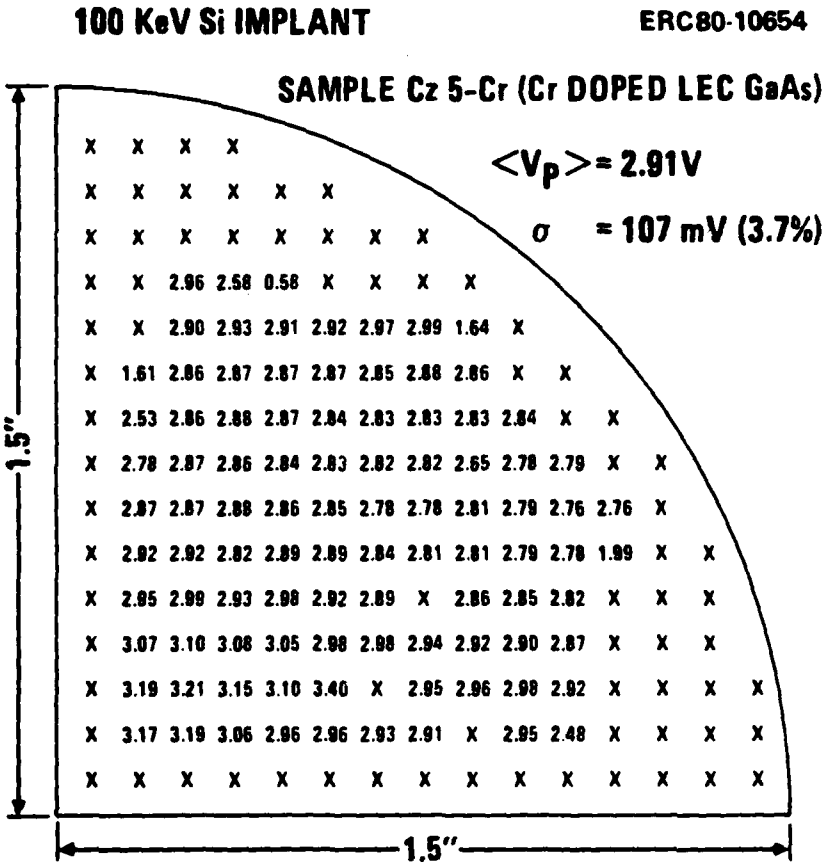


Fig. 3.7 Typical pinch-off voltage uniformity obtained on one quarter of a 3-in. Cr-doped LEC substrate.

Table 3.3-1

Active Layer Uniformity

Implant: 5E12 cm^{-2} 225 KeV Si

5E12 cm^{-2} 40 KeV Si

ID	Substrate Type	$\langle I_{dss} \rangle$ mA Before Gate Recess	σ (percent)
A	Undoped LEC	217.5	2.3
B	Undoped LEC	217.4	2.3
C	Undoped LEC	195.5	0.92
D	CR-doped Bridgman	193.4	2.0
E	CR-doped Bridgman	196.8	2.3
F	CR-doped Bridgman	201.0	4.4

$\langle I_{dss} \rangle$ = 203.6 mA

σ_{IDDS} = 11.0 mA (5.4%).

Table 3.3-2

Specific Contact Resistance Results

(After Completion of All MMIC Process Steps)

Date Measured	ID	Rc (Ω cm^2) $\times 10^6$
	Metallization: AuGe/Ni	
10/80	SP-100	0.51
	SP-101	0.66
	SP-102	1.31
	R2C-IL5	0.51
	15-2	0.99
	16-1	0.49
	W7-1	1.6
	W7-2	1.7
through	G19H-111	3.3
	W9-1	0.91
	W12-2	2.5
	W19-1	0.86
	60-1	3.1
	42-2	2.5
	40-1	0.56
	531	0.84
	711S421	0.30
	41-2	0.86
	511	1.1
5/82	T21	0.91
	$\langle R_c \rangle = 1.3 \times 10^{-6}\ \Omega\ cm^2$	
	$\sigma_{R_c} = 0.89 \times 10^{-6}\ \Omega\ cm^2$	

The uniformity, reproducibility, and dc yield of MIM capacitors has been studied. Uniformity and reproducibility data are given in Table 3.3-3. These data span a period of 20 months and clearly indicate that tight control of the PSN thickness and dielectric constant is obtained. Such control has encouraged the use of MIM capacitors for RF tuning as well as bypassing. The first group of data in Table 3.3-3 were obtained on wafers in process and the σ value reflects variations in both the PSN and the electroplated top electrode of the small (100 μm $\times$ 100 μm) test capacitors. Remaining data were obtained on

test wafers where the top electrode was formed by lift-off. Negligible variation in capacitance values was observed in these cases.

Table 3.3-3

MIM Capacitor Uniformity Data

Approx. Measurement Date	ID Number	Average Cap. pF/mm^2	σ (%)
6/80	143	125	2.1
	165	132	2.1
	173	132	3.4
	174	128	1.9
	175	131	2.4
	R5M/1B	125	1.8
	1265	135	3.2
	1357-1	127	*
	1357-2	133	*
	1393	125	*
	1398	125	*
	1412	125	*
through	1424	136	*
	1432	138	*
	1439	139	*
	1473	146	*
	1485	145	*
	1535	141	*
	1540	134	*
	1545	126	*
	1561	133	*
	1574	133	*
5/82	1612	137	*

Mean = 133 pF/mm^2, σ = 4.8%

*Less than the measurement accuracy

DC yield of MIM capacitors was found to depend on both the area and the length of overlap periphery (Fig. 3.8) between the first and the second metallization levels. A good fit of measured yield data to an equation of the form $Y = 1 - \alpha A - \beta P$ has been made using multiple linear regression. The equation terms are defined in Table 3.3-4. The last column of the table shows the contribution to circuit yield of 5 typical (10 pF) bypass capacitors and

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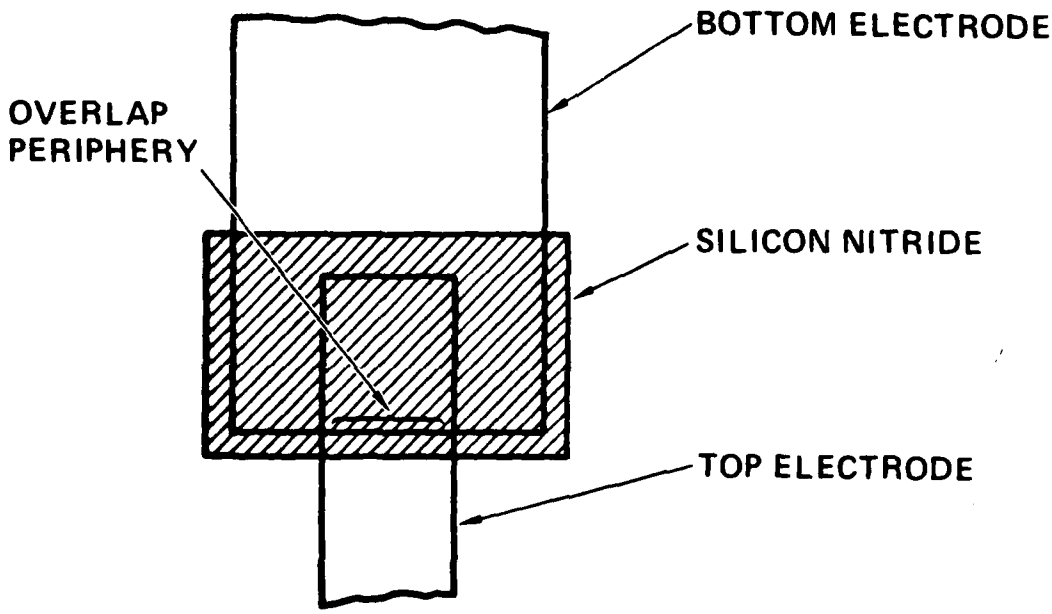

Fig. 3.8 Schematic diagram of a metal-insulator-metal (MIM) capacitor.

Table 3.3-4

DC Yield of MIM Capacitors

Insulator: 6000A Silicon Nitride Deposited by Plasma Etched CVD

$Y = 1 - \alpha A - \beta P$

Y = DC Yield

A = Capacitor Area (mm^2)

P = Overlap Periphery Between First and Second Metallization Levels (mm)

ID Number	α mm^{-2}	β mm^{-1}	RMS Prediction Error $\sqrt{\sum_i (y-y_i)^2}$	Yield of 10 pF Bypass Cap with Dimensions of A = 0.077 mm^2 P = 0.5 mm	Contribution to Circuit Yield Assuming 5 Bypass Capacitors
E	0.83	0.15	0.080	0.86	0.47
F	0.16	0.20	0.046	0.89	0.56
G	0.66	0.013	0.016	0.94	0.73

clearly indicates the importance of capacitor yield. The area dependence of capacitor yield is due to pinholes in the PSN. In practice, pinholes in the nitride are associated with debris on the wafer, metal splattering during first level metallization etc. and can be reduced by controlling these factors. The periphery dependence arises due to the sharp edges (as obtained by direct liftoff, Fig. 3.9a) which are not well covered by PSN and frequently result in a short. Rounded edges as obtained by the dielectric aided liftoff technique or ion milling (Fig. 3.9b) are more reliably covered by PSN and cause fewer shorts. Sample G in Table 3.3-4 had first level metal defined by ion milling and the data show a dramatic decrease in periphery related shorts by this processing approach. The periphery problem can be effectively circumvented by using an air bridge to contact the top capacitor electrode, but this approach adds to process complexity (unless air bridges are being used elsewhere in the circuit) and may constrain circuit layout.

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(a)

(b)

Fig. 3.9 (a) Sharp pattern edges obtained by direct liftoff of Ti(500Å)/Au(4000Å). (b) Smooth edges obtained by ion milling the metallization pattern.

After contact metallization, the 1.0 μm gates are defined by contact photolithography, recess etch, Ti-Pt-Au evaporation and liftoff. At present, gate yield is a significant circuit yield limiting factor. Some preliminary data is given in Table 3.3-5 where yields have been averaged over several wafers. The lower yield of 200 μm wide FETs as compared to the 500 μm wide FETs is due to the smaller source-drain gap of the 200 μm wide device. A significant increase in I_{dss} variation is observed after gate metallization. $\sigma_{I_{dss}}$ increased from ~ 5% before gate recess to ~ 17% after gate definition. This is attributed at present to the gate recessing process which is done by wet etching and is not well controlled. These data were obtained on ~ 10 cm^2 (half of a 2 in. wafer) GaAs wafers. Several precautions were taken to maximize gate yield including monitoring wafer flatness and ensuring that it is in the range of ± 1 μm/inch after capping and annealing, and using 0.090 inch thick masks for minimum runout due to mask bowing.

Table 3.3-5
FET DC Yield
$\langle I_{dss} \rangle$ = 43.4 mA (200 μm wide FET)
$\sigma_{I_{dss}}$ = 7.2 mA (16.6%)

Gate Periphery (μm)	200	500	990
Source-Drain Gap (μm)	3.8	4.8	4.8
FET Yield	87	92	88

Preliminary data on dc probe plus visual circuit yield of three different circuits is presented in Table 3.3-6. These data were obtained at the completion of front-end processing and do not include attrition due to subsequent steps involving thinning, via hole etching, backside metallization and sawing. The criterion "other processing defects" includes damage due to wafer handling, poor source-drain definition, and shorts caused by metallization

defects. The circuit yield data are commensurate with FET and capacitor yields presented earlier and represents some of the highest yields observed using the above described MMIC fabrication process, indicating the potential for achieving high overall yields of functional MMIC modules with subsystem complexity.

Table 3.3-6
DC Circuit Yield
$\langle I_{dss} \rangle$ = 43.4 mA (200 μm wide FET)
σ_{Idss} = 7.2 mA (16.6%)

	Buffer Amplifier	Driver Amplifier	Power Amplifier
Total Gate Periphery (mm)	0.2	1.0	1.98
Source-Drain Gap (μm)	3.8	4.8	4.8
Total MIM Capacitance (pF)	20	49.4	50.8
Gate Yield (%)	87	85	78
Capacitor Yield (%)	98	90	87
Plating Yield (%)	99	100	97
Yield Related to Other Processing Defects	94	90	88
DC Circuit Yield (%)	78	70	57

3.4 Circuit Fabrication Improvements for Low Noise

The fabrication approach described in previous sections was modified during the last phase of this program to obtain devices with lower noise figure and higher gain. The changes were aimed at reducing FET parasitics (gate metal resistance and gate-source resistance) while maintaining a gate length < 1 μm. This was accomplished by incorporating the following changes.

1. Gate-source resistance (R_{sg}) was reduced by forming a thin surface n^+ layer in the FET channel region in addition to the n^+ layer under the ohmic contacts. The channel sheet resistance was thus reduced to ~ 330 Ω/□ from ~ 1000 Ω/□ with a corresponding decrease in R_{sg}. The modified implant schedule was:

a. FET channel

Ion:	^{29}Si
Temperature:	~ 23°C (Room Temp.)
Dose:	3.5E12 cm^{-2}, 125 KeV
	5E12 cm^{-2}, 40 KeV

b. n^+ contact

Ion:	^{29}Si
Temperature:	~ 23°C (Room Temp.)
Dose:	1E13 cm^{-2}, 250 KeV

The wafers were capped and annealed as described previously. Before gate metallization, the active layer was recessed through the gate photoresist mask by chemical etching. I_{dss} of a 200 μm wide FET was monitored as a function of recess depth and etching was terminated when a current of 60 ± 5 mA was reached.

2. Gate metallization was changed from Ti-Pt-Au to W-Au while keeping metal thickness constant at 6500Å. The W was then selectively etched in a CF_4 plasma to obtain an undercut, T-shaped structure shown schematically in Fig. 3.4-1. This fabrication approach permits submicron gates by using 1.0 μm FET technology while overcoming the usual problem of high gate resistance of submicron gates formed by direct liftoff. Gate resistance is lowered here by the large cross section of this structure.

The two changes described above were incorporated in the last two wafer lots which resulted in significant improvements in both dc and RF characteristics of devices and the 8 GHz low noise amplifier. Typical reduction observed in R_{sg} is as shown in Table 3.4-1. This is also reflected in low knee voltage of FET dc characteristics (Fig. 3.4-2). The LNA performance is described in Section 4.1 and FET characteristics are described in Section 4.2.

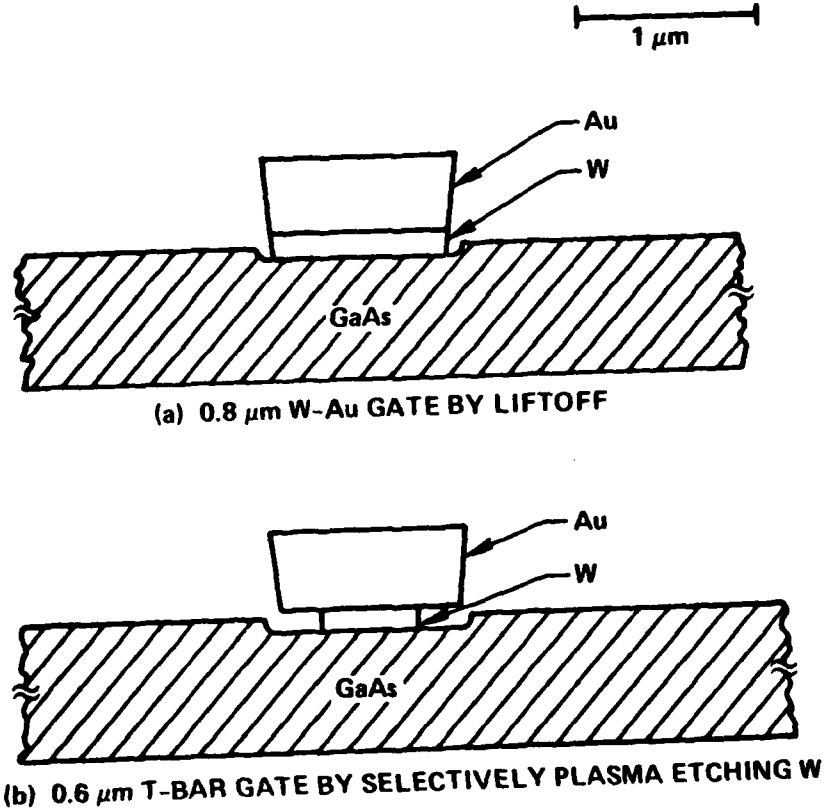
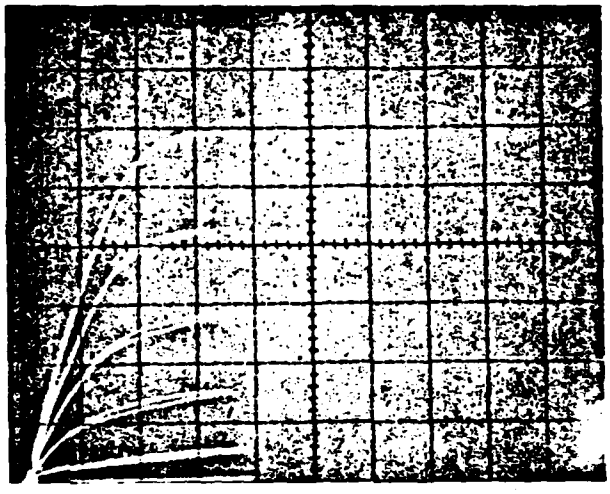


Fig. 3.4-1 W-Au gate with T shaped cross section.



GATE PROCESS: T-BAR, W-Au (Recessed)
GATE WIDTH: 300 μm

SCALE: 10 mA/DIV (VERT.)
0.5 V/DIV (HORZ.)
0.5 V/STEP.

Fig. 3.4-2 Recessed gate FET d-c characteristics.

Table 3.4-1

Effect of Surface N^+ Layer

Gate Length = 1.0 μm

Gate Width = 200 μm (End Fed)

Source-Drain Gap = 3.8 μm

Wafer ID	Surface n^+	Average Source-Gate Resistance (ohms)	Average Source Contact Resistance (ohms)	Calculated (from Cols. 3 and 4) Sheet Resistance (ohms/square)
A	No	8.9	2.0	986
B	Yes	3.9	1.5	343

4.0 CHARACTERIZATION AND TEST RESULTS

Measurement techniques and test results for the latest circuits are presented in Section 4.1. Section 4.2 then describes the active device measurement technique needed to adequately model monolithic circuits and presents performance data on the FETs used in this program. Section 4.3 concludes with an analysis of the measured data and a comparison with predicted results. Recommendations for further work in this area are contained in Section 5.0.

4.1 Measured Performance Results

Characterization of Monolithic Microwave Integrated Circuits required careful fixturing to minimize the parasitic effects of the test set which might mask true device performance. The test fixture used initially (shown in Fig. 2.4) provides most of the required characteristics. Connection to the automatic network analyzer is made via OSM coaxial to microstrip transitions. Fifty ohm microstrip transmission lines on alumina substrate then provide an RF path directly to the MMIC input and output bonding pads. DC bias is supplied through spring loaded bias clips (bypassed with low frequency capacitors) to the microstrip RF chokes on the alumina substrates. Bond wires then connect the bias chokes to the monolithic chip, and optional bypass chip capacitors can be included if desired. Most of the dc bias circuitry on the test fixture is not needed for MMIC testing since on-chip bypass capacitors are provided in all of the circuits developed for this program. They are included for additional testing flexibility during circuit evaluation. Chip carrier and alumina substrate can be easily interchanged for testing different chips, and minor modifications provide the ability to test chips of a different size.

One modification of this test fixture was found necessary while testing the initial circuits. The ground plane discontinuity due to machining tolerances can occasionally produce resonant effects at the interface between the alumina substrate and the chip carrier bar. Careful machining and judicious use of indium foil provided a temporary solution to this problem, however, the new circuits were tested in a modified fixture. In the new fixture the carrier bar extends under the alumina substrate to provide a continuous ground plane up

to the GaAs chip. In both designs the chip is recessed to place the top of the alumina and GaAs substrate in the same plane, thereby minimizing bond wire inductive effects.

The intermediate frequency amplifier was characterized in the fixture described above, and the measured gain is shown in Fig. 4.1. The gain is approximately 3.5 dB higher than predicted in Fig. 2.3 because the 100 ohm input shunting resistor was deleted in the new design as described in Section 2.3. Measured gain is in excellent agreement with predicted gain of the improved circuit. As shown in Fig. 4.2, output match is excellent both across the band and well out of the band due to the broadband active matching of the common drain (or source follower) output stage. The input directly feeds the gate-to-source capacitance of the dual gate FET, which is negligible at the IF frequency. Therefore, the input is almost an open circuit as shown in Fig. 4.2.

The improved 8 GHz preamplifier was fabricated and characterized with two different FETs. The changes in the active device center around the minimization of parasitic source resistance by a gate recess process as described in Section 3.4. Initial results (without gate recess) are shown in Figs. 4.3 and 4.4. Noise figures of 5.3, 5.5, and 4.2 dB were measured at 6.5, 7.5, and 8.5 GHz, respectively. Associated gain in excess of 7 dB was obtained from this single stage amplifier, and gain above 9 dB is available at a higher bias current.

Single stage preamplifiers with improved active devices were also characterized. As expected, substantial improvements in noise performance were achieved as shown in Fig. 4.5. These chips were fabricated with thick ground planes which reduced circuit losses and further enhanced noise performance.

Characterization of the two-stage amplifier also produced excellent agreement between measured and predicted results. Figure 4.6 shows the measured gain and noise figure of the two-stage preamplifier without gate recess processing. Figure 4.7 shows the excellent input and output match. Note that the noise performance is similar to that expected from cascading two of the single stage amplifiers with performance shown in Fig. 4.3. Bias cannot be adjusted on this chip to optimize gain performance since the resistance bias

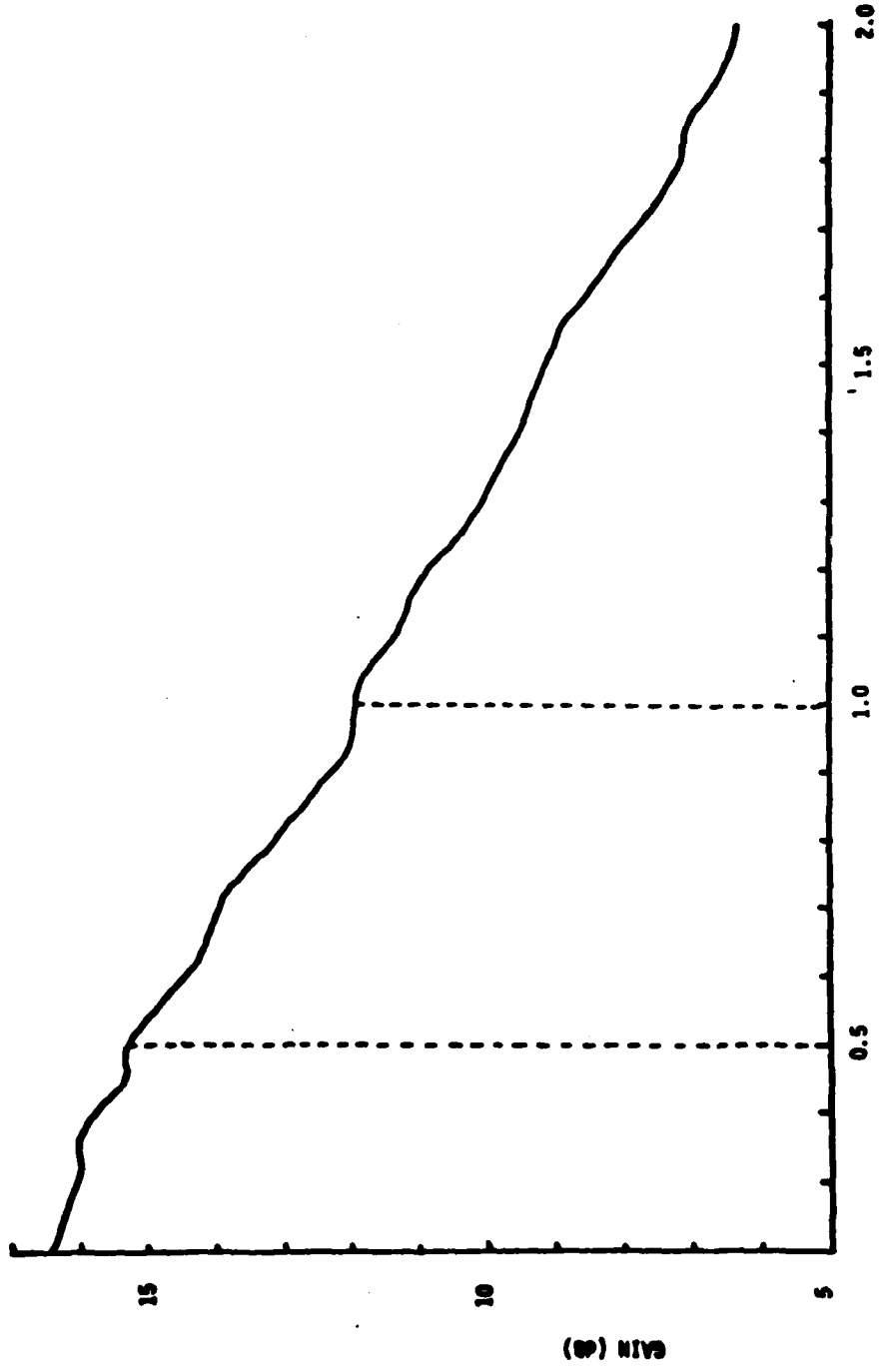


Fig. 4.1 Measured gain of the improved IF amplifier.

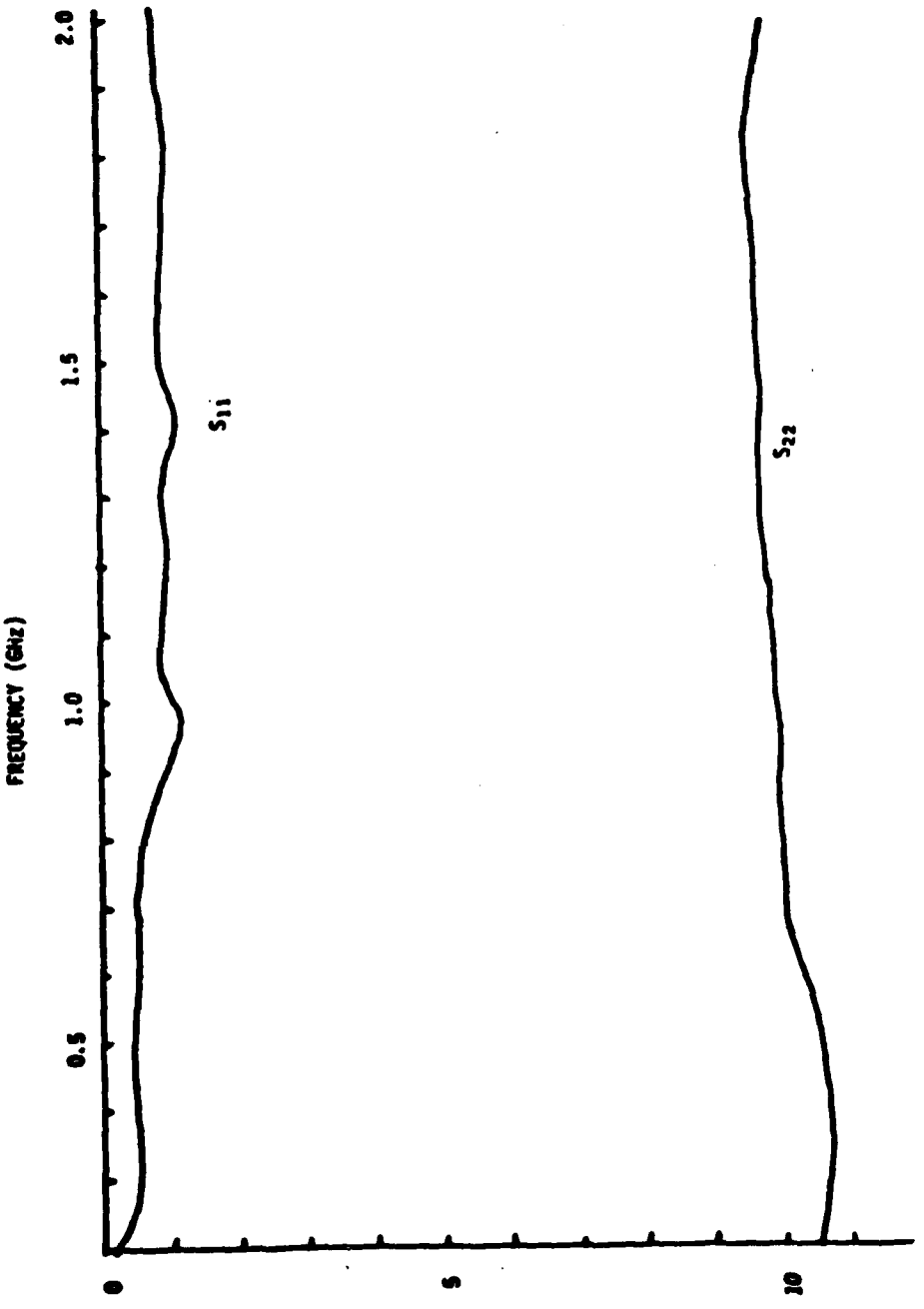


Fig. 4.2 Measured input and output match of the improved IF amplifier.

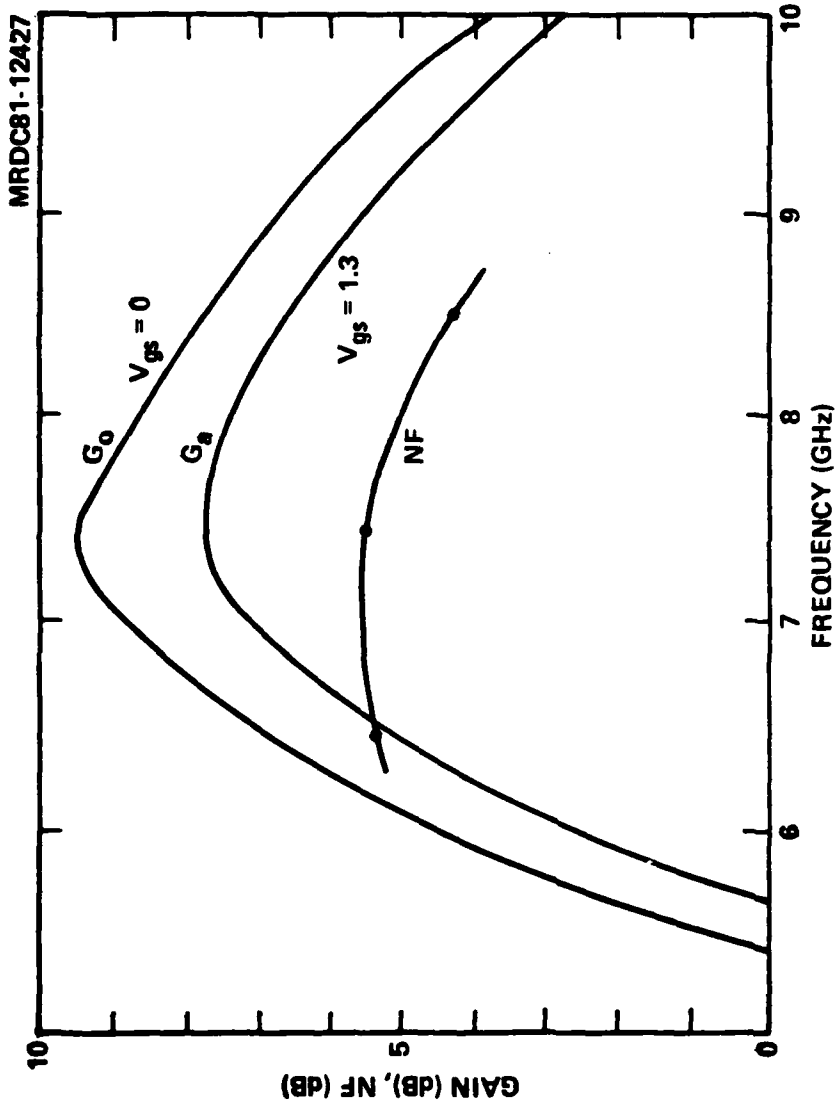


Fig. 4.3 Measured preamplifier gain and noise figure without gate recess.

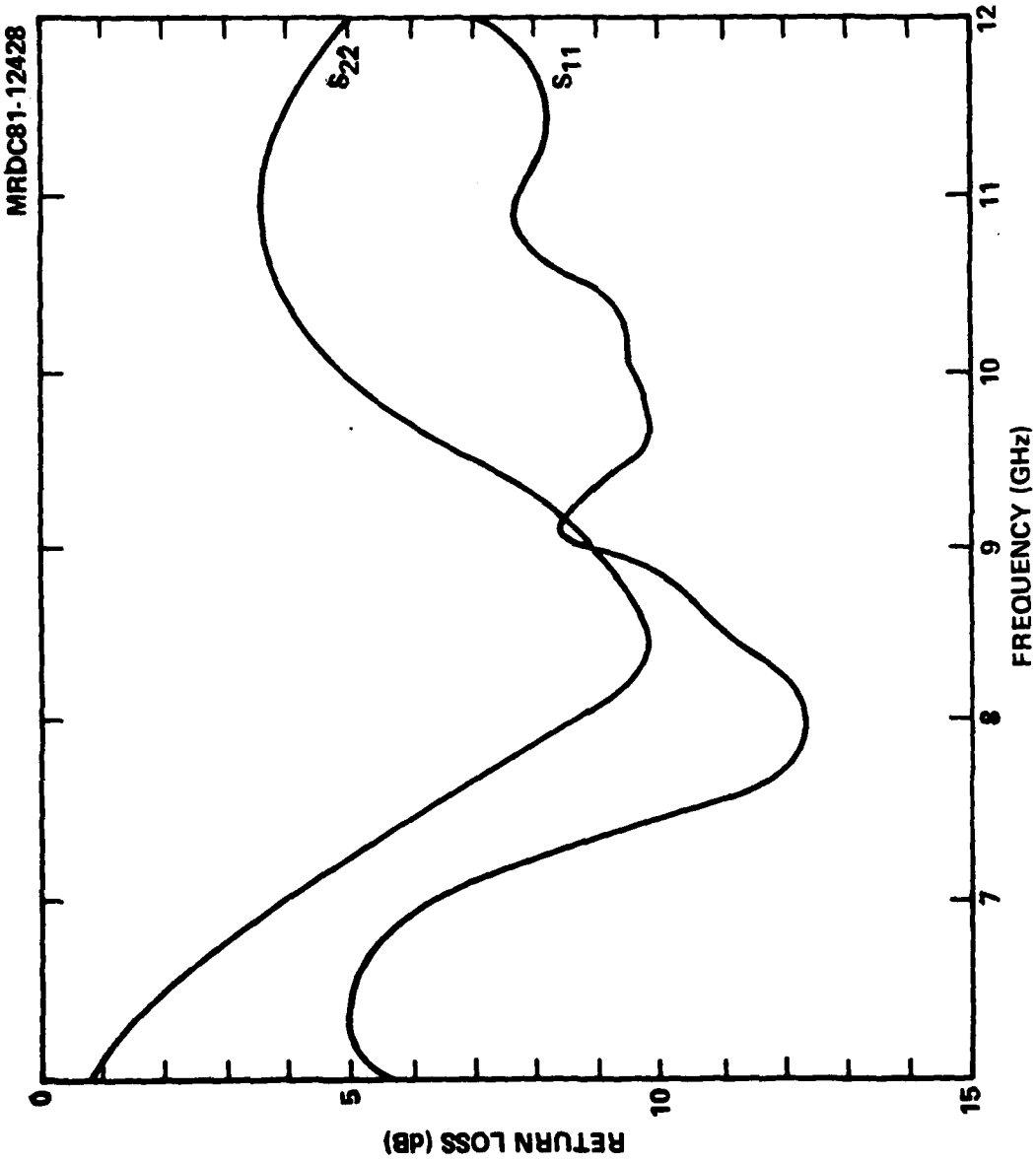


Fig. 4.4 Measured preamplifier input and output match.

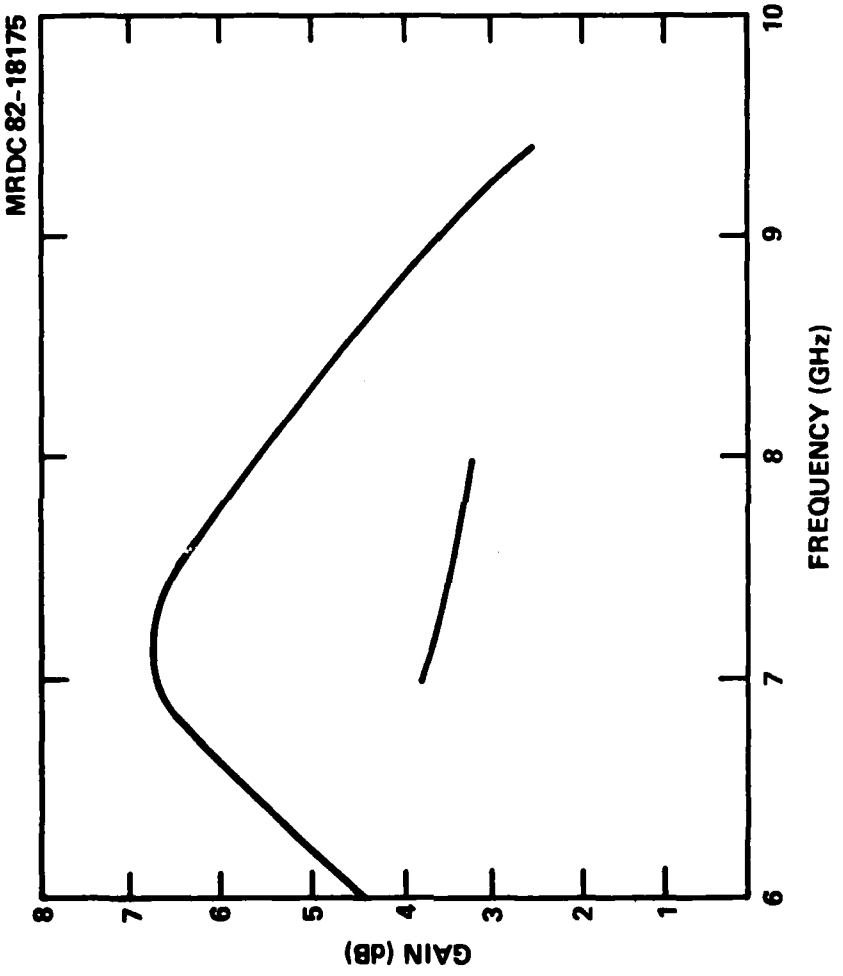


Fig. 4.5 Measured preamplifier gain and noise figure with gate recess.

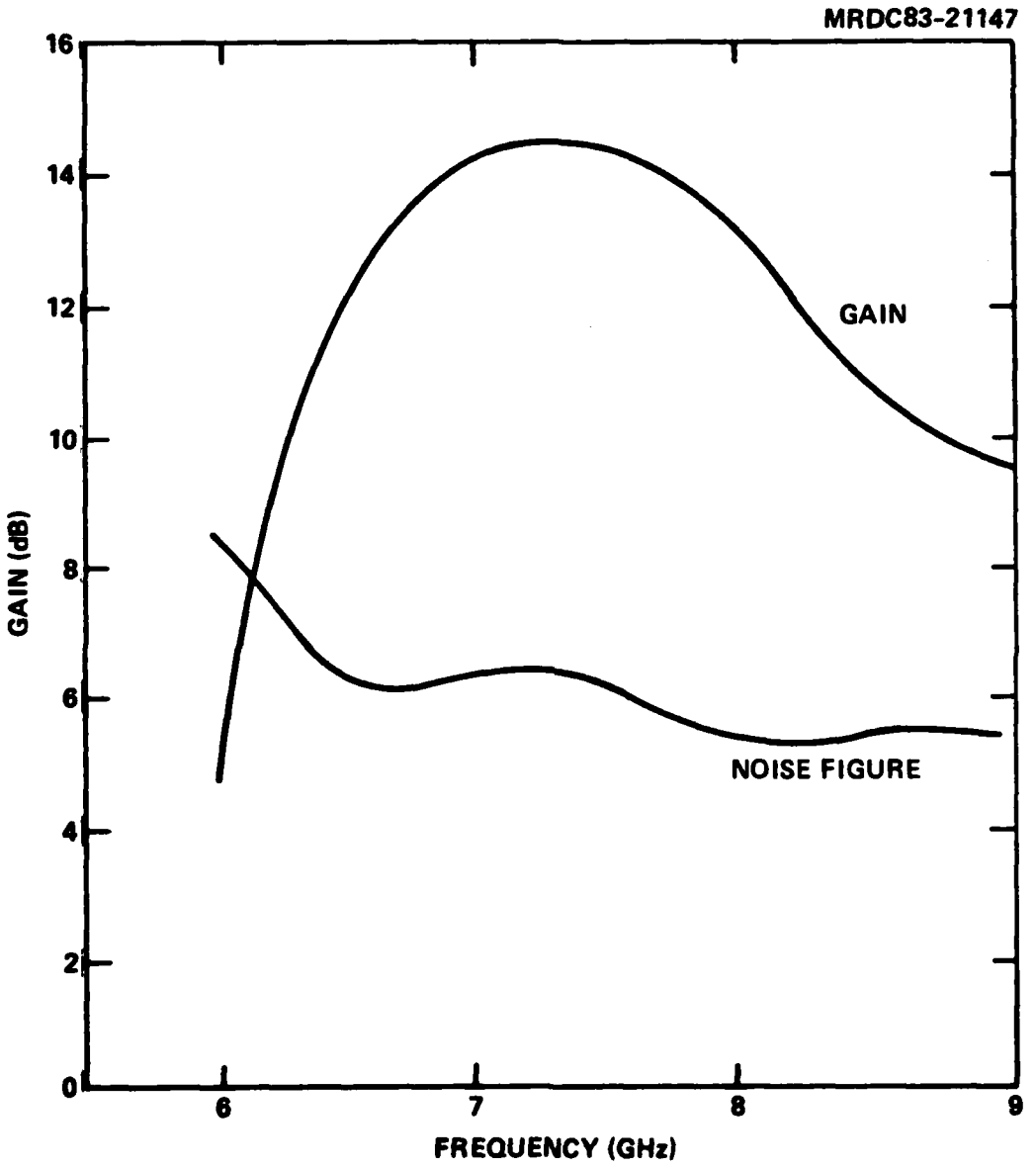


Fig. 4.6 Gain and noise figure of the two-stage buffer amplifier without gate recess.

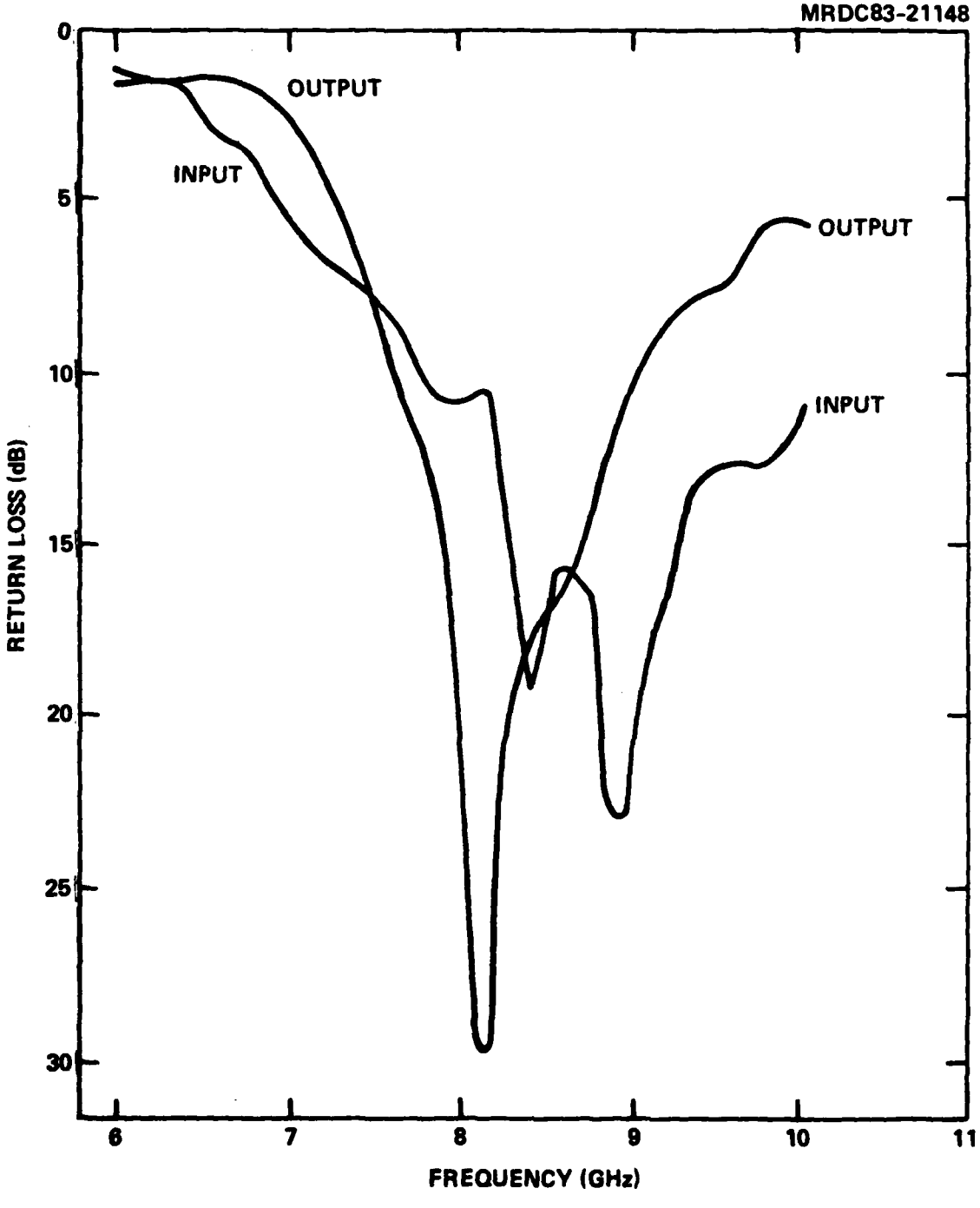


Fig. 4.7 Input and output match of the two-stage buffer amplifier.

network is an integral part of the monolithic circuit as shown in Fig. 2.20. Unfortunately, the inclusion of on-chip bias resistors also precludes the testing of a gate recessed two-stage preamplifier without the generation of additional mask levels. Since FET active layers and resistors are formed in the same process step for this mask set, all resistors are significantly reduced in value for the same reason parasitic resistances of the FET are minimized. Under the assumption that performance would be similar to a cascade of two single stage amplifiers, a noise figure of 3.8 dB with an associated gain of 11.8 dB can be expected at 8 GHz from this circuit and gate recess processing.

The monolithic voltage controlled oscillator operated as expected except that the operating frequency was slightly high and output power was quite low. The free running oscillator frequency (with 0 volts across the varactor capacitance) varied from device to device but always occurred between 9.5 and 10.5 GHz. Oscillator performance is marginal as indicated by the low output power (approximately -15 dBm) and the lack of oscillation in several devices. Those devices which did not oscillate became operational when the buffer amplifier was disconnected by scribing its inductive input line. Without the buffer amplifier load impedance, the free running frequency of operation was approximately 11 GHz. Note that the 100 ohm source resistance is still present in this mode of operation. Tuning either the gate-to-source capacitance, C_{gs}, or the varactor diodes resulted in a tuning range of approximately 100 MHz. The narrow tuning range and high operating frequency indicate that the resonant circuit is not presenting an optimum impedance to the gate of the oscillator FET. Either inaccuracies in the varactor model, the FET model, or both are the likely causes of this discrepancy. The inductive transmission lines have been used in many previous designs and are modeled quite accurately, though models of stray coupling and distributed ground effects are still in need of improvement.

The gain of the buffer amplifier cannot be measured experimentally since it is an integral part of the monolithic chip. There is no input bonding pad and it is not matched to 50 ohms at the input. It is possible to measure the output match, which is shown in Fig. 4.8 and agrees well with theoretical prediction.

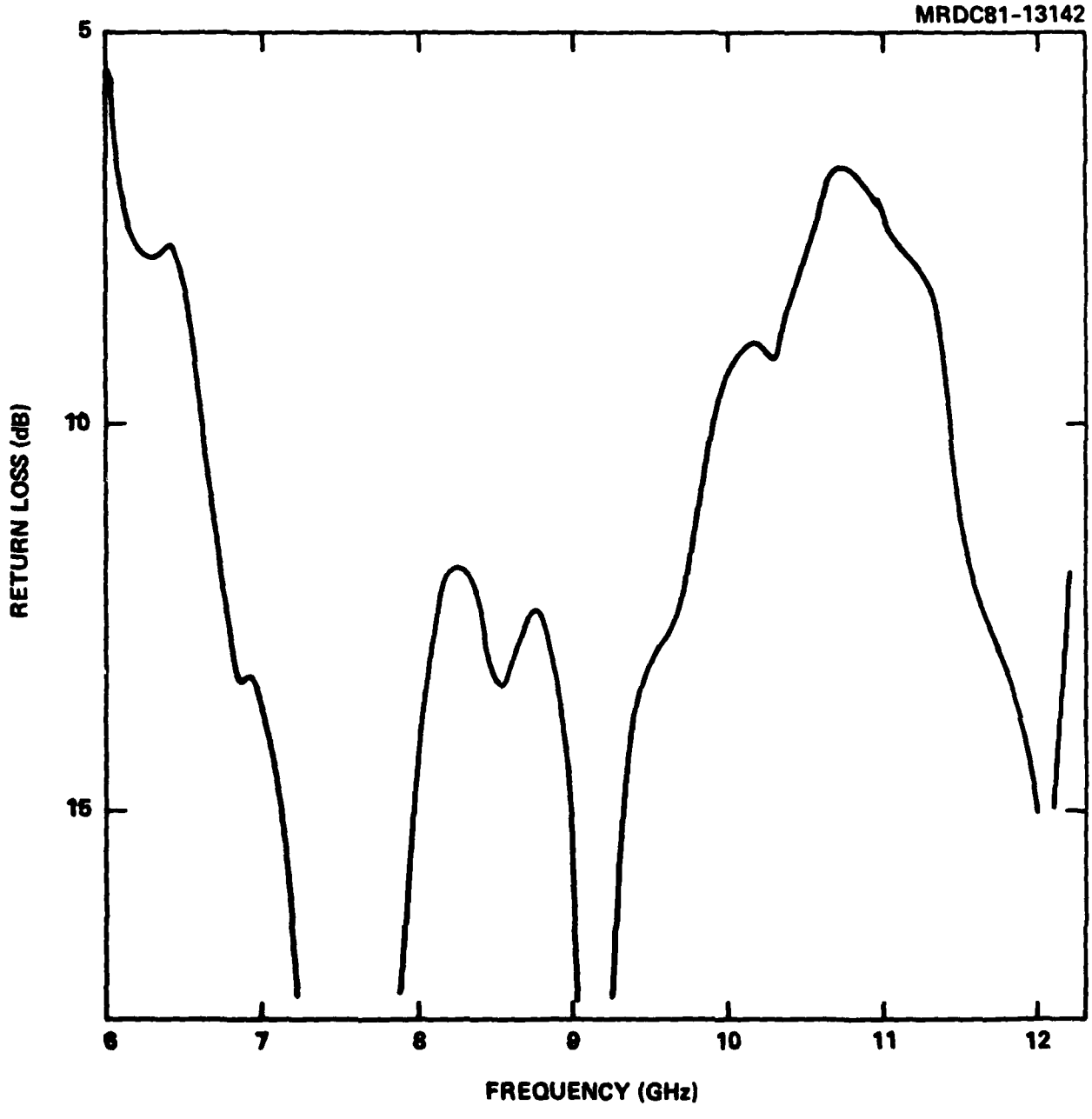


Fig. 4.8 Measured output return loss of the buffered local oscillator.

Mixer performance similarly suffers from inaccurate nonlinear device modeling. Conversion loss of approximately 6 dB can routinely be obtained, however, better performance requires the use of external tuning elements. This circuit requires the most effort for improvement, but a useful receiver can be fabricated with the existing device if the loss is compensated by additional gain in the preamplifier or intermediate frequency amplifier sections of the receiver.

4.2 Characterization of Active Devices

The mask set used to fabricate the monolithic receiver circuits contains discrete FETs to facilitate device characterization. Since these FETs are fabricated simultaneously with the circuits, they are very similar to the active devices used in the MMICs and their characterization provides valuable diagnostic and design information. Sample chips from the wafer are mounted in low noise FET packages for evaluation. DC measurements are carried out as outlined by Fukui* to determine FET parameters such as R_g (gate metal resistance), R_{sg} (gate-source resistance), R_{gd} (gate-drain resistance), L_{eff} (effective gate length), g_m (transconductance), etc. 1 MHz capacitance measurements are made to determine C_{gs} versus V_{gs}. These data, along with g_m versus V_{gs} curves provide useful diagnostic information since they can be correlated to measured amplifier input match as a function of gate bias. Noise figure measurements are made to obtain actual noise data and results are checked against noise figure calculations from dc parameters obtained earlier as outlined by Fukui.

*H. Fukui, "Determination of the Basic Device Parameters of a GaAs MESFET," B.S.T.J., Vol. 58, No. 3, pp. 771-797, March 1979.

Using the diagnostic tools described above, several changes in device parameters became apparent when the process was modified as outlined in Section 3.4. A significant drop in R_{gs} was observed as already indicated in Table 3.4-1. This was accompanied by a substantial increase in external transconductance (g_m) from ~ 80 ms/mm to ~ 120 ms/mm and in C_{gs} (0) from ~ 1.67 pF/mm to ~ 2.4 pF/mm. f_T calculated from

$$f_T = \frac{g_m}{2\pi C_{gs}}$$

increased slightly from 7.6 GHz to 8.0 GHz. Although no significant change in f_T was observed, the noise performance of the new devices is better because of reduced parasitic resistances. This is seen both from the measured performance and the following equation from Fukui paper:

$$F_{min} = 10 \log \left[1 + kfL \sqrt{\frac{g_m(R_g + R_{gs})}{1 - g_m R_s}}\right]$$

where f is the frequency in GHz, L is the gate length in μm and g_m (Ω^{-1}) is measured at the noise bias K is a constant whose value is approximately 0.27.

The increase in $C_{gs}(0)$ indicates a higher surface doping in the new devices. This might have been expected in view of the shallow FET implant (peak doping at only 1000Å) and a surface n^+ implant. Some devices have been made (using a different mask set) with a deeper FET implant (peak at ~ 2000Å) in conjunction with a surface n^+ layer. Preliminary mesurements of C_{gs} (0) show a value of 1.38 pF/mm which is lower than that from a single implant. It therefore appears that by judicious selection of implantation parameters the desired C_{gs} value can be obtained. This is important since circuit performance is intimately tied to FET input capacitance. For instance, the LNA input match at 8 GHz deteriorated with the new devices because of high input capacitance of the FET. However, as previously mentioned, noise figure was improved due to reduced parasitic resistances.

4.3 Performance Analysis

Analysis of the initial linear circuits (RF and IF amplifiers), careful layout considerations for parasitic element minimization, and inclusion of an improved FET fabrication technology have led to successful fabrication of full performance RF and IF amplifier circuits. Although the two-stage buffer amplifier could not be fabricated with improved active devices using the existing mask set, conversion of the mask set for processing compatibility is straightforward. Full performance monolithic two stage buffer amplifiers would then be available for integration on the receiver chip.

Measurement of the non-linear components of the receiver indicate that a similar circuit analysis, design and layout modification, and fabrication iteration must still be performed to reach full performance. Key to successful implementation of the non-linear circuits is the availability of accurate non-linear element models and associated computer algorithms for efficient circuit simulation. Combined with the improved device fabrication techniques and layout experience gained under this program, a strong non-linear analysis capability will lead to a fully functional monolithic receiver front end on GaAs.

5.0 SUMMARY AND RECOMMENDATIONS

The three year effort described in this report lead to several functional components and paved the way for a wide range of monolithic circuits based on the technology developed. A single stage and two stage low noise amplifier were successfully developed along with an intermediate frequency amplifier. All are process compatible with final monolithic integration of a Monolithic Gallium Arsenide Superheterodyne Front End. Initial results on a monolithic mixer are encouraging, however, more development work is needed prior to final integration. An 8 GHz oscillator was under development for a companion contract and is also suitable for inclusion in the final configuration.

It is recommended that development work continue on the mixer while further improving noise performance of the preamplifiers. This work would culminate in final integration of an 8 GHz superheterodyne front end. The component approach with input and output aligned for final interconnection has worked well in the past and is recommended for future development programs.